



**SOUTH AFRICAN MICRO-ELECTRONIC SYSTEMS (PTY) LTD**  
 33 ELAND STREET, KOEDOESPOORT, P.O. BOX 15888, LYNN EAST, PRETORIA, 0039  
 TEL: (+27 12) 333-6021 \ FAX: (+27 12) 333-8071  
**Web site:**

<http://www.sames.co.za>

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## Procedure

<b>Title:</b> <b>PROCESS DATA SHEET FOR C1015</b>		<b>Doc Number</b> WF-J004-002 <b>Revision:</b> 1
<b>Department:</b> Manufacturing  <b>Area:</b> BIP Yield  <b>Process:</b> C1015	<b>Approved &amp; Released Procedure</b>	
<b>Document Type:</b> PROCESS DATA SHEETS		<b>Retention Period:</b> 5 - Year(s) <b>Review Period -</b> 365 Days

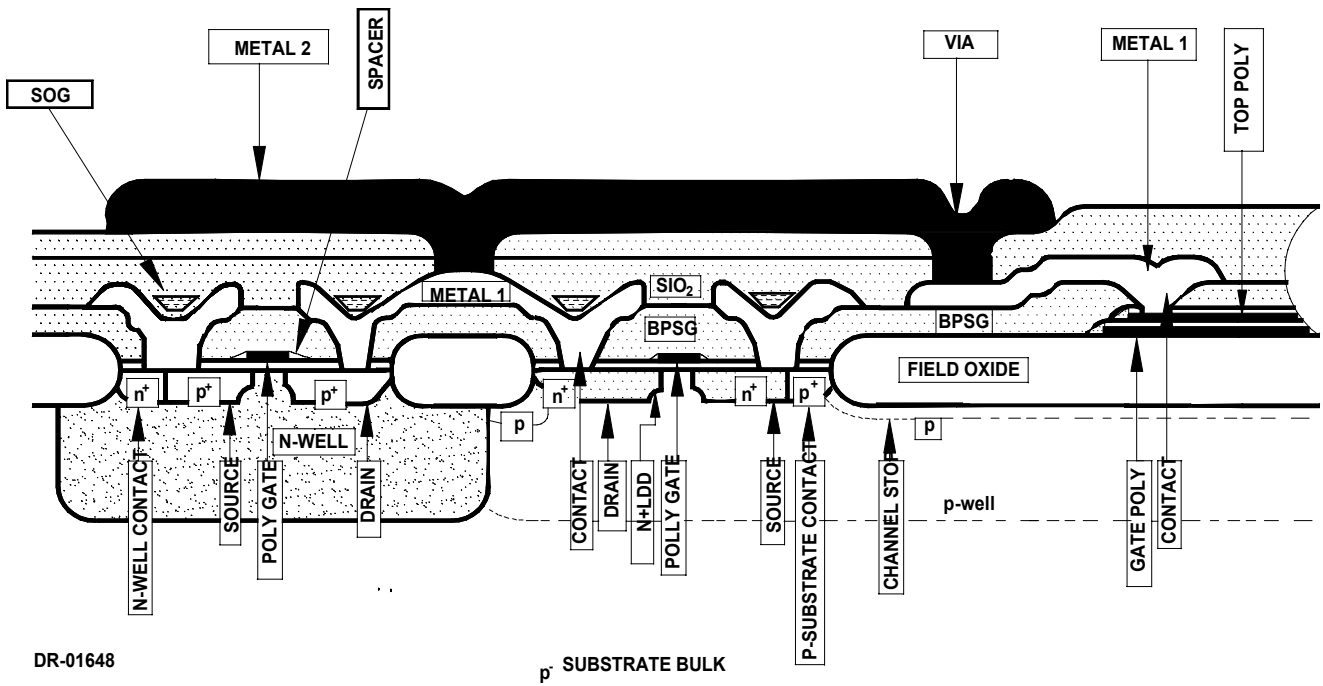
### 1.0 micron CMOS, Double Metal, Double Poly Process

#### Physical Characteristics

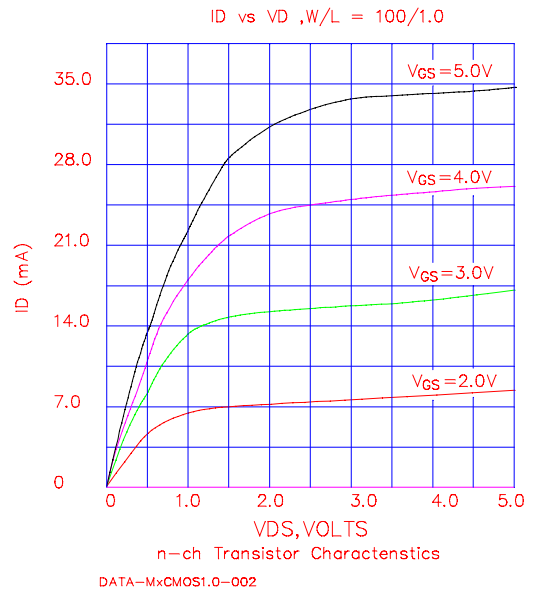
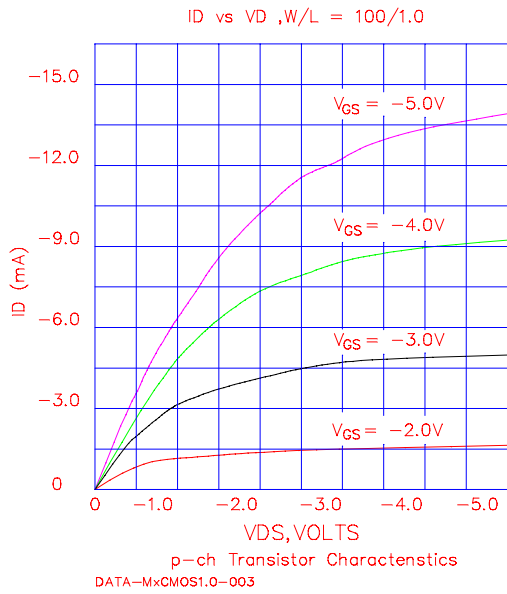
<b>Process Geometry</b>	1.0 micron
<b>Process Number</b>	C1015
<b>Operating Voltage</b>	5V ± 10%
<b>Well Doping</b>	N-WELL
<b>Metal Layers</b>	2
<b>Poly Layers</b>	2
<b>Contact</b>	1.2 µm
<b>Via</b>	1.2 µm
<b>Metal I Width</b>	1.4 µm
<b>Metal I Space</b>	1.2 µm

<b>Metal II Width</b>	1.8 µm
<b>Metal II Space</b>	1.4 µm
<b>Gate Poly Width</b>	1.0 µm
<b>Gate Poly Space</b>	1.4 µm
<b>N+ / P+ Width</b>	2.0 µm
<b>N+ / P+ Space</b>	1.2 µm
<b>N+ to N-WELL</b>	5.0 µm
<b>N+ to P+</b>	7.0 µm

### CROSS SECTIONAL VIEW OF THE CMOS 1.0 PROCESS



DR-01648



**N-ch transistor**

(T = +25°C unless otherwise noted)

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	$V_{TO_N}$	0.65	0.85	1.05	V	25 x 1.0 $\mu\text{m}$ device
Body Factor	$\gamma_N$	0.77	0.87	0.97	$V^{1/2}$	25 x 1.0 $\mu\text{m}$ device
Conduction Factor (normalized)	$\beta_N$	38	41.5	45	$\mu\text{A}/V^2$	25 x 25 $\mu\text{m}$ device
Effective Channel Length	$L_{eff_N}$	0.75	0.95	1.15	$\mu\text{m}$	25 x 1.0 $\mu\text{m}$ device
Width Encroachment	$\Delta W_N$		0.4		$\mu\text{m}$	Per side
Punch Through Voltage	$BVDSS_N$	8.0			V	25 x 1.0 $\mu\text{m}$ device
Poly Field Threshold	$V_{TFP_N}$	8.0			V	

**P-ch transistor**

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	$V_{TO_P}$	-1.2	-1.0	-0.8	V	25 x 1.0 $\mu\text{m}$ device
Body Factor	$\gamma_P$	0.46	0.56	0.66	$V^{1/2}$	25 x 1.0 $\mu\text{m}$ device
Conduction Factor (normalized)	$\beta_P$	12.0	13.5	15.0	$\mu\text{A}/V^2$	25 x 25 $\mu\text{m}$ device
Effective Channel Length	$L_{eff_P}$	0.75	1.0	1.25	$\mu\text{m}$	25 x 1.0 $\mu\text{m}$ device
Width Encroachment	$\Delta W_P$		0.45		$\mu\text{m}$	Per side
Punch Through Voltage	$BVDSS_P$			-8.0	V	25 x 1.0 $\mu\text{m}$ device
Poly Field Threshold	$V_{TFP_P}$			-8.0	V	

**Diffusion & Thin films**

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Well (field) Sheet Resistance	$R_{s_{N-(f)}}$	0.7	1.0	1.3	$\text{k}\Omega/$	N-well
N+ Sheet Resistance	$R_{s_{N+}}$	27	37	47	$\Omega/$	
N+ Junction Depth	$X_{jN+}$		0.4		$\mu\text{m}$	
P+ Sheet Resistance	$R_{s_{P+}}$	70	90	110	$\Omega/$	
P+ Junction Depth	$X_{jP+}$		0.4		$\mu\text{m}$	
Gate Poly Sheet Resistance	$R_{s_{POLY(N)}}$	25	32	39	$\Omega/$	
Metal 1 Sheet Resistance	$R_{s_{M1}}$		50		$\text{m}\Omega/$	
Metal 2 Sheet Resistance	$R_{s_{M2}}$		30		$\text{m}\Omega/$	

**Capacitance**

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Gate Oxide	$C_{OX}$	1.57	1.72	1.92	$\text{fF}/\mu\text{m}^2$	
Metal 1 to Poly	$C_{M1P}$		0.046		$\text{fF}/\mu\text{m}^2$	
Metal 2 to Metal 1	$C_{MM}$		0.038		$\text{fF}/\mu\text{m}^2$	
Poly1 to Poly2	$C_{P1-P2}$	0.42	0.52	0.616	$\text{fF}/\mu\text{m}^2$	