

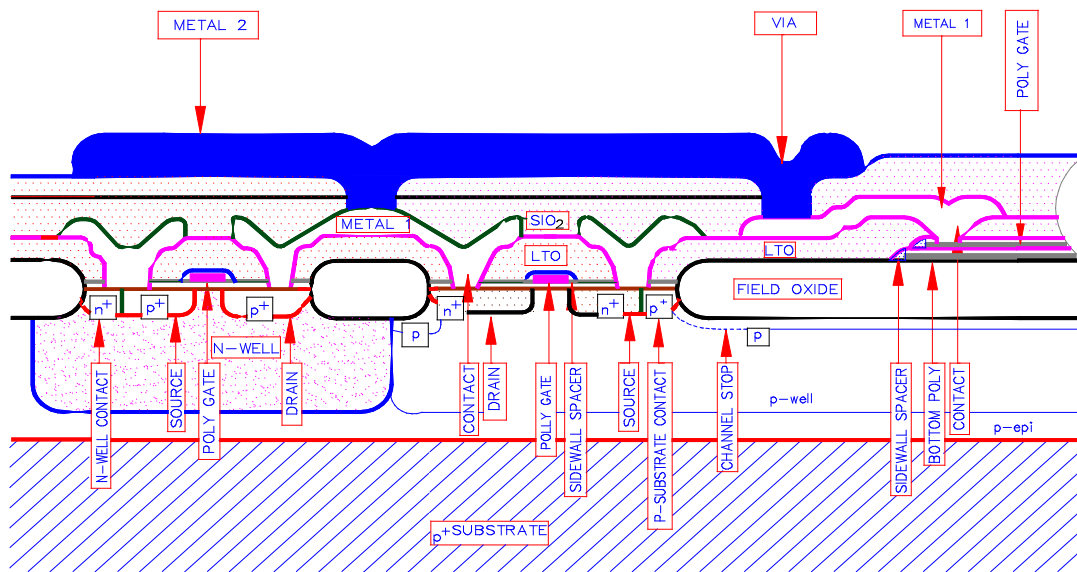


CMOS1.2 PROCESS

PHYSICAL CHARACTERISTICS

Process Geometry	1.2 micron
Process Number	C1201(S.P/D.M)/ C1202(D.P/D.M)
Operating Voltage	5v
Well Doping	N-WELL
Metal Layers	2
Poly Layers	1/2
Contact	1.5 μ
Via	1.5 μ
Metal I Width	2.0 μ
Metal I Space	2.0 μ

Metal II Width	2.0 μ
Metal II Space	2.0 μ
Gate Poly Width	1.2 μ
Gate Poly Space	1.8 μ
Bottom Poly Width	3.0 μ
Bottom Poly Space	2.0 μ
N+/P+ Space	2.0 μ
N+ to N-WELL	7 μ
N+ to P+	9 μ



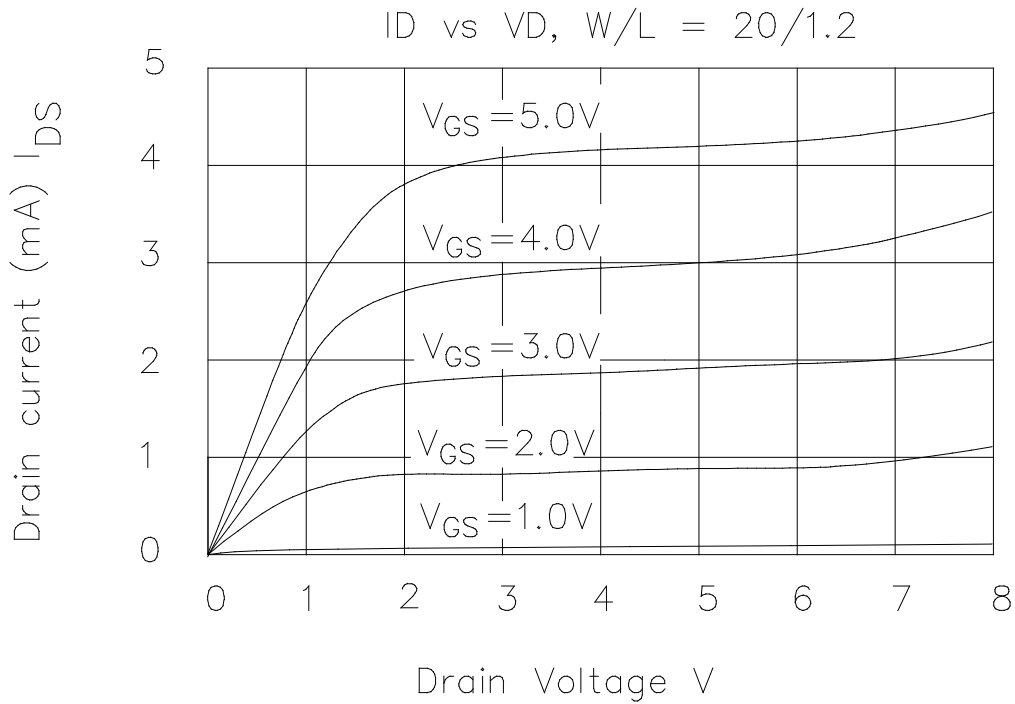
DR-00031

CROSS SECTIONAL VIEW OF THE CMOS 1.2 PROCES

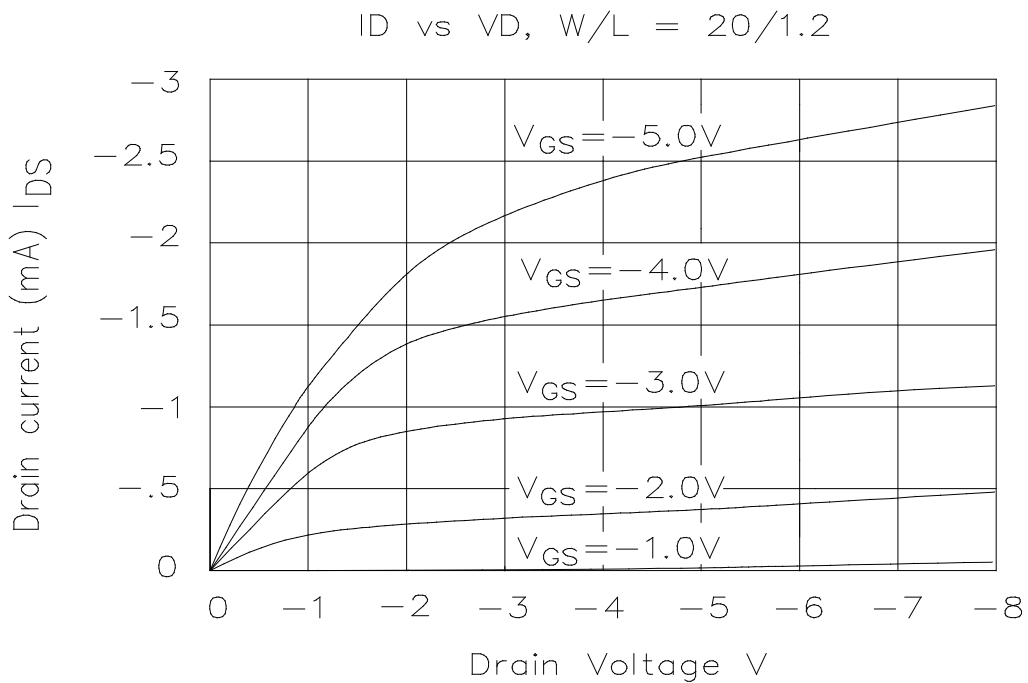


CMOS1.2 PROCESS

N-CH transistor IV characteristics of a 20/1.2 device.



P-CH transistor IV characteristics of a 20/1.2 device.





CMOS1.2 PROCESS

ELECTRICAL CHARACTERISTICS

n-ch transistor

(T = +25°C unless otherwise noted)

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	VTON	0.55	0.75	0.95	V	100/1.2 device
Body Factor	Y _N		0.35		V ^{1/2}	100/1.2 device
Conduction factor (normalized)	β _N	64	75	86	μA/V ²	100/100 device
Effective Channel Length	LEFF _N	0.85	1.15	1.3	μm	100/1.2 device
Width Encroachment	ΔW _N		0.6		μm	per side
Punch Through Voltage	BVDSS _N	9			V	100/1.2 device
Poly Field Threshold	VTF _{P(N)}	10			V	
Threshold Voltage Offset (two sigmas)	ΔVTF _N		5		mV	100/10 device

p-ch transistor

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	VTOP	-1.1	-0.9	-0.7	V	100/1.2 device
Body Factor	Y _P		0.4		V ^{1/2}	100/1.2 device
Conduction Factor (normalized)	β _P	20	25	30	μA/V ²	100/100 device
Effective Channel Length	LEFF _P	0.95	1.25	1.4	μm	100/1.2 device
Width Encroachment	ΔW _P		0.6		μm	per side
Punch Through Voltage	BVDSS _P			-8	V	100/1.2 device
Poly Field Threshold	VTF _{P(P)}			-10	V	
Threshold Voltage Offset (two sigmas)	ΔVTF _P		5		mV	100/10 device



CMOS1.2 PROCESS

diffusion & thin films

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Well (field) Sheet Resistance	$R_{W(+)}$	0.7	1	1.2	$k\Omega/$	n-well
N+ Sheet Resistance	R_{N+}	20	30	50	$\Omega/$	
N+ Junction Depth	X_{JN+}		0.4		μm	
N-Well Junction Depth	X_{jnw}		0.3		μm	
P+ Sheet Resistance	R_{P+}	50	80	100	$\Omega/$	
P+ Junction Depth	X_{JP+}		0.3		μm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	18	25	32	$\Omega/$	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	15	25	50	$\Omega/$	
Bottom Poly Sheet Resistance	R_{POLYB}	20	25	37	$\Omega/$	
Metal 1 Sheet Resistance (SLM)	R_{M1}		30		$m\Omega/$	
Metal 1 Sheet Resistance (DLM)	R_{M2}		50		$m\Omega/$	
Metal 2 Sheet Resistance (DLM)	R_{M2}		30		$m\Omega/$	

capacitance

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Poly Gate to Bottom Poly	C_{PP}		0.86		$fF/\mu m^2$	interpoly capacitor
Metal 1 to Poly	C_{M1P}		0.057		$fF/\mu m^2$	
Metal 2 to Metal 1	C_{MM}		0.035		$fF/\mu m^2$	