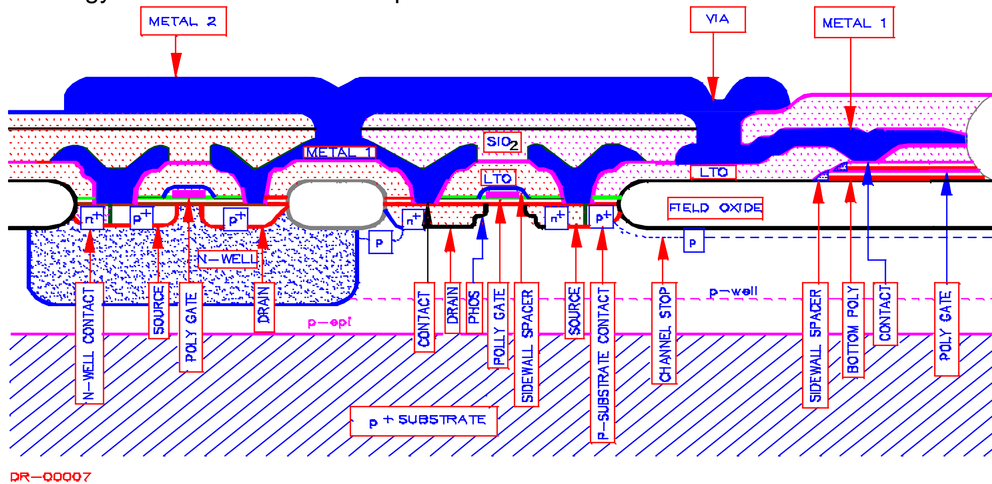
sames

3CMOS 1,2 Process

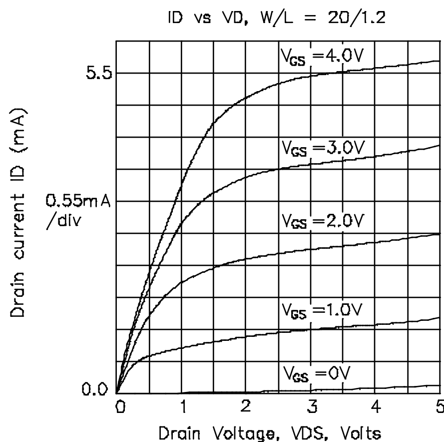
Physical Characteristics

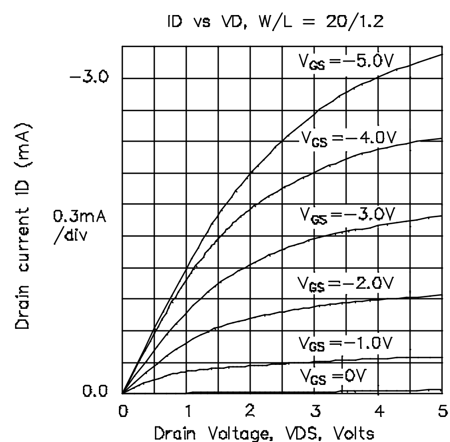
Parameter	Value	Parameter	Value
Process Geometry	1.2 Micron	Metal II Width	2.5μ
Process Number	C1210	Metal II Space	1.5μ
Operating Voltage	5V	Gate Poly Width	1.5μ
Well Doping	N-WELL	Gate Poly Space	2.0μ
Metal Layers	2	Bottom Poly Width	3.0μ
Poly Layers	2	Bottom Poly Space	2.0μ
Contact	1.5μ	N+/P+ Width	2.5μ
Via	1.5μ	N+/P+ Space	2.0μ
Metal I Width	2.5μ	N+ to N-WELL	7.0μ
Metal I Space	1.5μ	N+ to P+	9.0μ

Note: This process provides zero V_T transistors in addition to standard V_T transistor of 1.2μm technology. Refer to 3CMOS 1.2 process data sheet.



CROSS-SECTIONAL VIEW OF THE 3CMOSS1.2 PROCESS





3CMOS 1,2 Process

Electrical Characteristics

n-ch transistor (T = +25°C unless otherwise noted)

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (linear extrapolated)	VTO_N	0.05	0.15	0.3	V	100/1.2 device
Body Factor	γ_N	.29	0.36	.44	$V^{1/2}$	100/1.2 device
Conduction factor (normalized)	β_N	75	90	105	$\mu A/V^2$	100/100 device
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	µm	100/1.0 device
Width Encroachment	ΔW_N		0.6		µm	per side
Punch Through Voltage	$BVDSS_N$	9			V	100/1.0 device
Poly Field Threshold	$VTF_{P(N)}$	10			V	
Threshold Voltage Offset (two Sigmas)	ΔVT_N		5		mV	100/10 device

p-ch transistor

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (linear extrapolated)	VTO_P	-0.2	0.0	0.2	V	100/1.2 device
Body Factor	γ_P	0.4	0.5	0.7	$V^{1/2}$	100/1.2 device
Conduction Factor (normalized)	β_P	18	23	28	$\mu A/V^2$	100/100 device
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	µm	100/1.2 device
Width Encroachment	ΔW_P		0.8		µm	per side
Punch Through Voltage	$BVDSS_P$			-9	V	100/1.2 device
Poly Field Threshold	$VTF_{P(P)}$			-10	V	
Threshold Voltage Offset (two Sigmas)	ΔVTP		5		mV	100/10 device

diffusion & thin films

Parameters	Sym	Min	Typ	Max	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N-(f)}$	0.8	1.4	2.0	kΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	X_{jN+}		0.30		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	X_{jP+}		0.30		µm	
Gate Poly Sheet Resistance (n-ch)	$\rho_{POLY(N)}$	15	22	30	Ω/□	
Bottom Poly Sheet Resistance	ρ_{M1}		35		mΩ/□	
Metal 1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal 2 Sheet Resistance	ρ_{M2}		30		mΩ/□	

capacitance

Parameters	Sym	Min	Typ	Max	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Poly Gate To Bottom Poly	C_{pp}		0.86		$fF/\mu m^2$	Interpolycapacitor
Metal 1 to Poly	C_{M1p}		.046		$fF/\mu m^2$	
Metal 2 to Metal 1	C_{MM}		.035		$fF/\mu m^2$	