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 Procedure		
Title: PROCESS DATA SHEET FOR C1219		Doc Number PROC-1191 Revision: 4
Department: Manufacturing Area: BIP Yield Process: C1219	<i>Approved & Released Procedure</i>	
Document Type: PROCESS DATA SHEETS Standard Element:		Retention Period: - None Review Period - Days



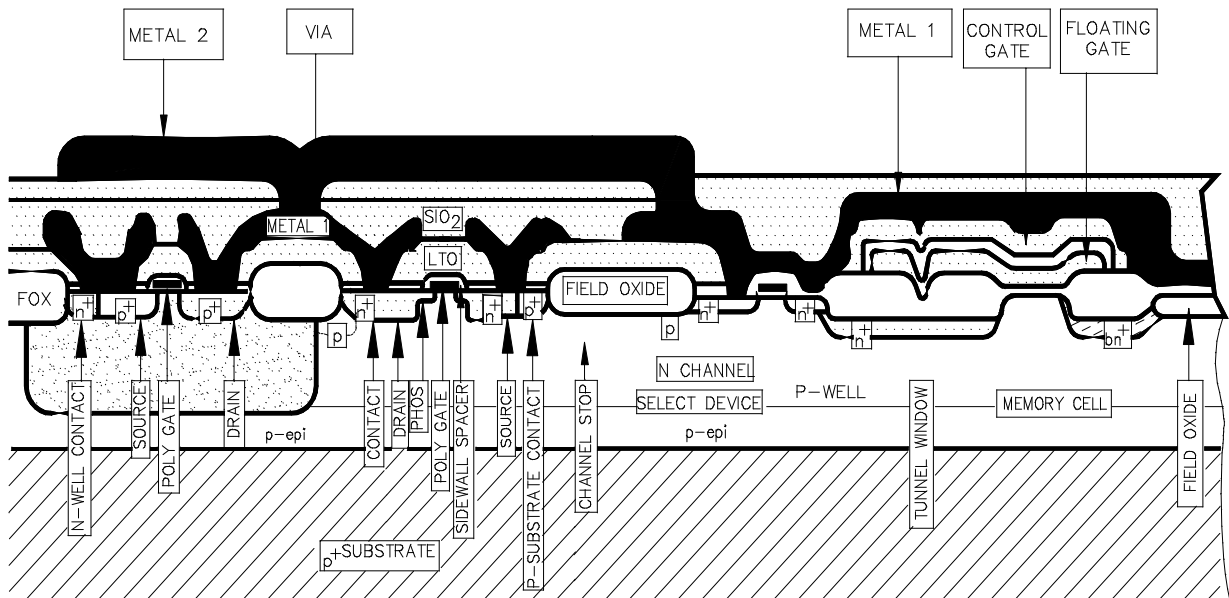
EECMOS 1.2 PROCESS WITH HIGH RESISTIVE POLY AND LOW THRESHOLD TRANSISTORS

PHYSICAL CHARACTERISTICS

Process Geometry	1.2 micron
Process Number	C1219
Operating Voltage	3V
Well Doping	TWIN-WELL
Metal Layers	2
Poly Layers	2
Contact	1.5 μ
Via	1.5 μ
Metal I Width	2.5 μ
Metal I Space	1.5 μ

Metall II Width	2.5 μ
Metal II Space	1.5 μ
Gate Poly Width	1.5 μ
Gate Poly Space	2.0 μ
Bottom Poly Width	3.0 μ
Bottom Poly Space	2.0 μ
N+ / P+ Width	2.0 μ
N+ / P+ Space	2.0 μ
N+ to N-WELL	7.0 μ
N+ to P+	9.0 μ

CROSS SECTIONAL VIEW OF THE EECMOS 1.2 PROCESS



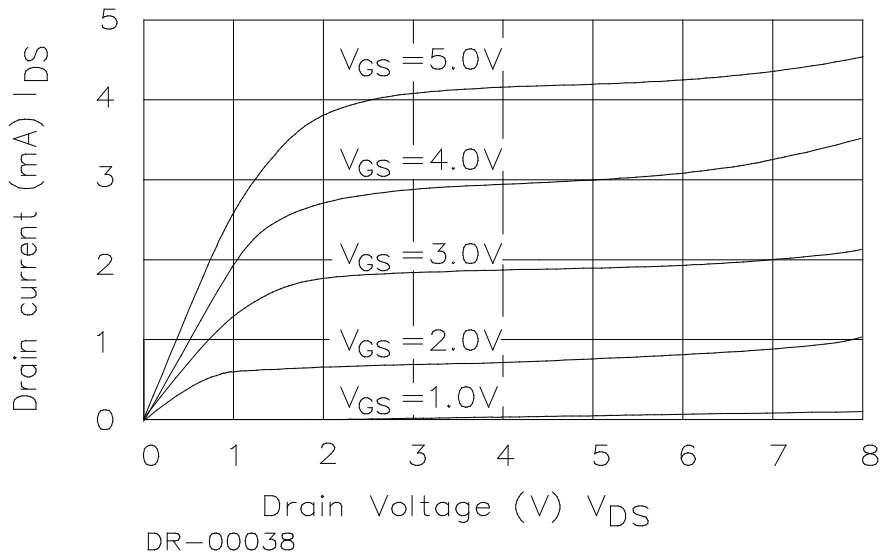
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EECMOS 1.2 PROCESS WITH HIGH RESISTIVE POLY AND LOW THRESHOLD TRANSISTORS

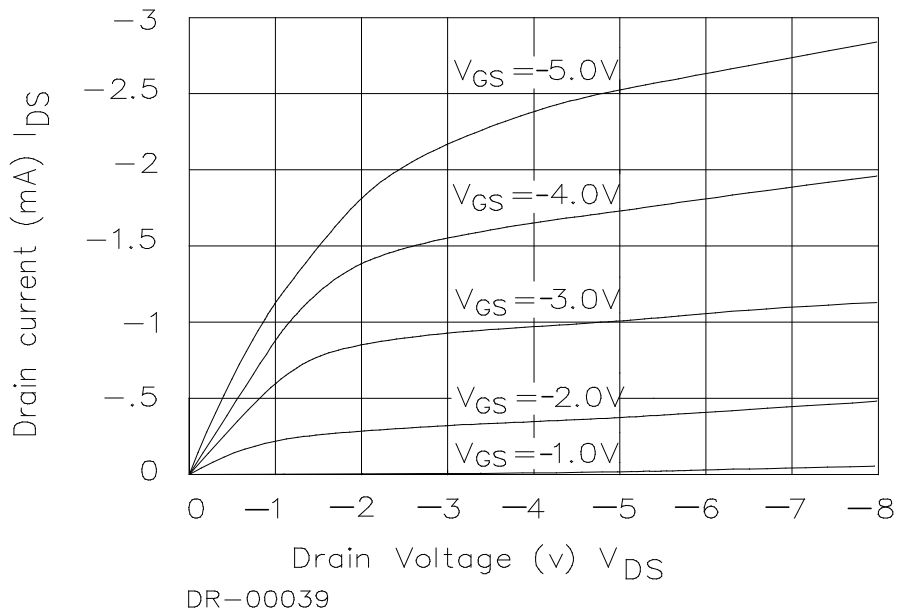
n-ch transistor IV characteristics of a 20/1.2 device

I_D vs V_D , $W/L = 20/1.2$



p-ch transistor IV characteristics of a 20/1.2 device

I_D vs V_D , $W/L = 20/1.2$





EECMOS 1.2 PROCESS WITH HIGH RESISTIVE POLY AND LOW THRESHOLD TRANSISTORS

ELECTRICAL CHARACTERISTICS

n-ch transistor

T = +25°C unless otherwise noted

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	V_{TO_N}	0.30	0.475	0.65	V	100/1.2 device
Body Factor	Y_N	0.35	0.45	0.55	$V^{1/2}$	100/1.2 device
Conduction factor (normalized)	B_N	64	78	92	$\mu A/V^2$	100/100 device
Effective Channel Length	L_{eff_N}	0.8	1.0	1.2	μm	100/1.2 device
Width Enroachment	ΔW_N		0.6		μm	per side
Punch Through Voltage	$BVDSS_N$	5			V	100/1.2 device
Poly Field Threshold	$VTF_{P(N)}$	8			V	
Threshold Voltage Offset (two Sigmas)	ΔVT_N		5		mV	100/10 device

p-ch transistor

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	V_{TO_P}	-0.65	-0.475	-0.3	V	100/1.2 device
Body Factor	Y_P	0.5	0.6	0.7	$V^{1/2}$	100/1.2 device
Conduction Factor (normalized)	B_P	20	25	30	$\mu A/V^2$	100/100 device
Effective Channel Length	L_{eff_P}	0.9	1.1	1.3	μm	100/1.2 device
Width Enroachment	ΔW_P		0.8		μm	per side
Punch Through Voltage	$BVDSS_P$			-5	V	100/1.2 device
Poly Field Threshold	$VTF_{P(P)}$			-8	V	
Threshold Voltage Offset (two Sigmas)	ΔVT_P		5		mV	100/10 device

EECMOS Characteristics

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Tunnel Thickness	$t_{TUNNEL\ OX}$		90		Å	
Interpoly Oxide Thickness	$T_{INTERPOLY\ OX}$		400		Å	
Buried N+ sheet Resistance	Rho_{BM+}		300		$\Omega/[]$	
Initial Program / Erase Window			6		V	
Umpogrammed Memory Threshold	VT		17		V	
Endurance			10^5		Cycles	
Programming Votlage	V_{PP}		13		V	



EECMOS 1.2 PROCESS WITH HIGH RESISTIVE POLY AND LOW THRESHOLD TRANSISTORS

diffusion & thin films

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Well (field) Sheet Resistance	$Rho_{N-(f)}$	1.2	2.0	2.8	$k\Omega/$	n-well
N+ Sheet Resistance	Rho_{N+}	20	35	50	$\Omega/$	
N+ Junction Depth	X_{JN+}		0.30		μm	
P+ Sheet Resistance	Rho_{P+}	50	75	100	$\Omega/$	
P+ Junction Depth	X_{JP+}		0.30		μm	
Gate Poly Sheet Resistance	$Rho_{POLY(N)}$	15	22	30	$\Omega/$	
Bottom Poly Sheet Resistance	Rho_{M1}		35		$m\Omega/$	
High Resistive Poly Sheet Resistance	Rho_{POLYH}	1.5	2.0	2.5	$k\Omega/$	
Metal 1 Sheet Resistance	Rho_{M1}		50		$m\Omega/$	
Metal 2 Sheet Resistance	Rho_{M2}		30		$m\Omega/$	

capacitance

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Poly Gate to Bottom Poly	C_{PP}		0.86		$fF/\mu m^2$	interpoly capacitor
Metal 1 to Poly	C_{M1P}		0.057		$fF/\mu m^2$	
Metal 2 to Metal 1	C_{MM}		0.035		$fF/\mu m^2$	

Associated Documents:

Documents Generated:

Document Title	Responsibility	Department

Document Revision History:

Revision: 4	Date Created: 04-10-2002 Date of Last Revision: 07-06-2004	Last Approval Date: 07-06-2004
Document Author: Ettiene Smit	Document Manager: Alan Sasnovski	

Reason for Change:

Revision:	Sec/Para Changed	Change Made:	Date
1	N/A	Initial Issue of Document	4-10-02
2		Added page breaks	29-10-02
3		Change Process description to add Low Threshold Transistors and changed the Electrical Characteristics	16-01-03
4	Physical Characteristics	Change Well doping from N-Well to Twin-Well	04-06-04

Electronic Notification List:

Approvals:

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