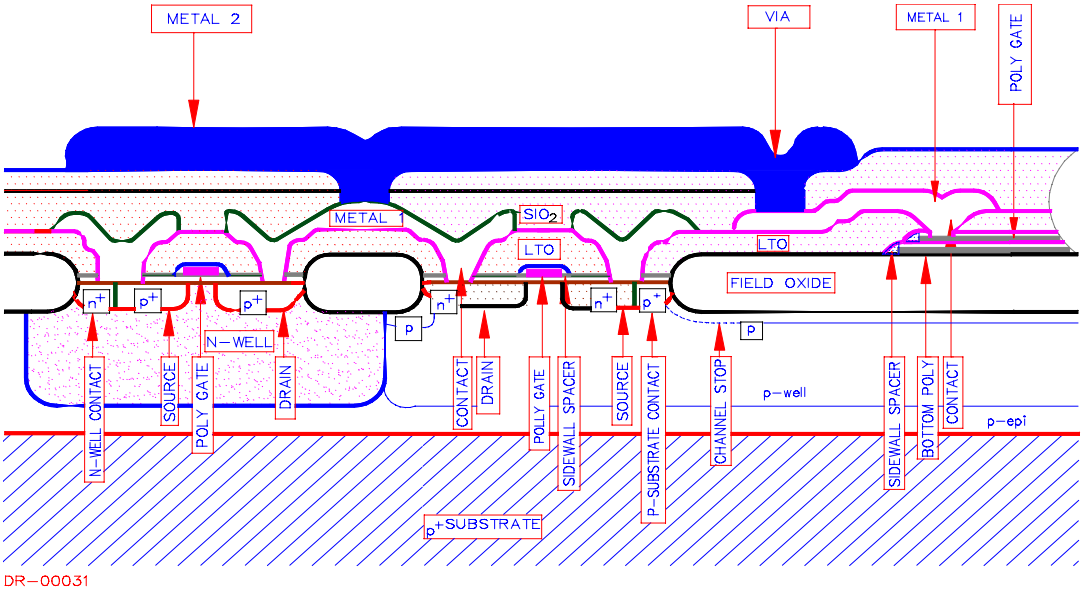
HV CMOS1.2 PROCESS

PHYSICAL CHARACTERISTICS

Process Geometry	1.2 micron
Process Number	C1221(H.V/S.P/D.M)
Operating Voltage	35v
Well Doping	N-WELL
Metal Layers	2
Poly Layers	1
Contact	1.5 µ
Via	1.5 µ
Metal I Width	2.0 µ
Metal I Space	2.0 µ

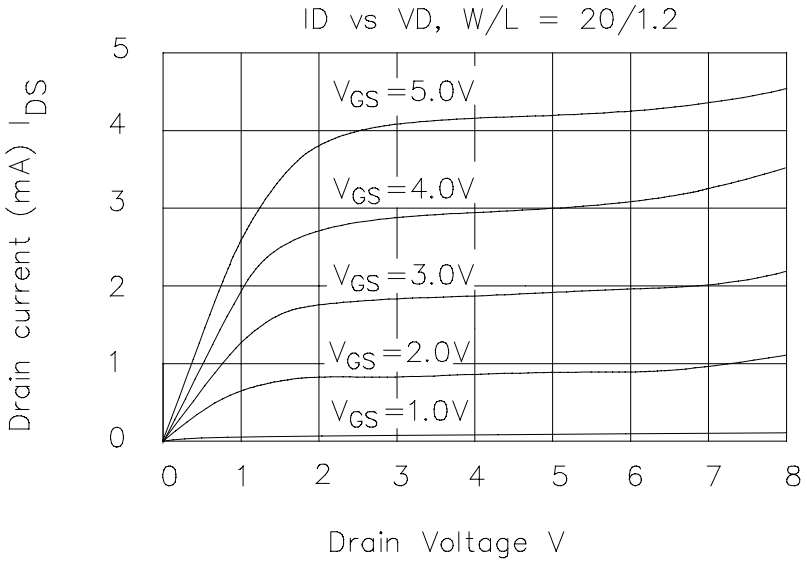
Metal II Width	2.0 µ
MetalI II Space	2.0 µ
Gate Poly Width	1.2 µ
Gate Poly Space	1.8 µ
Bottom Poly Width	3.0 µ
Bottom Poly Space	2.0 µ
N+/P+ Space	2.0 µ
N+ to N-WELL	7 µ
N+ to P+	9 µ



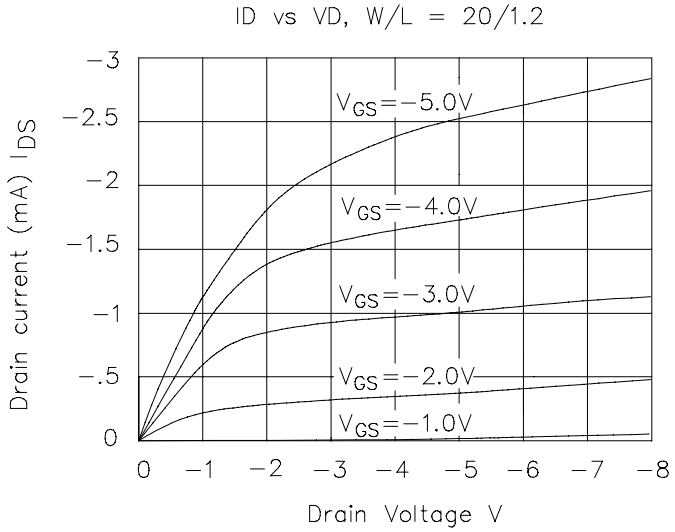
CROSS SECTIONAL VIEW OF THE CMOS 1.2 PROCESS

HV CMOS1.2 PROCESS

N-CH transistor IV characteristics of a 20/1.2 device. (VDS = 5V)

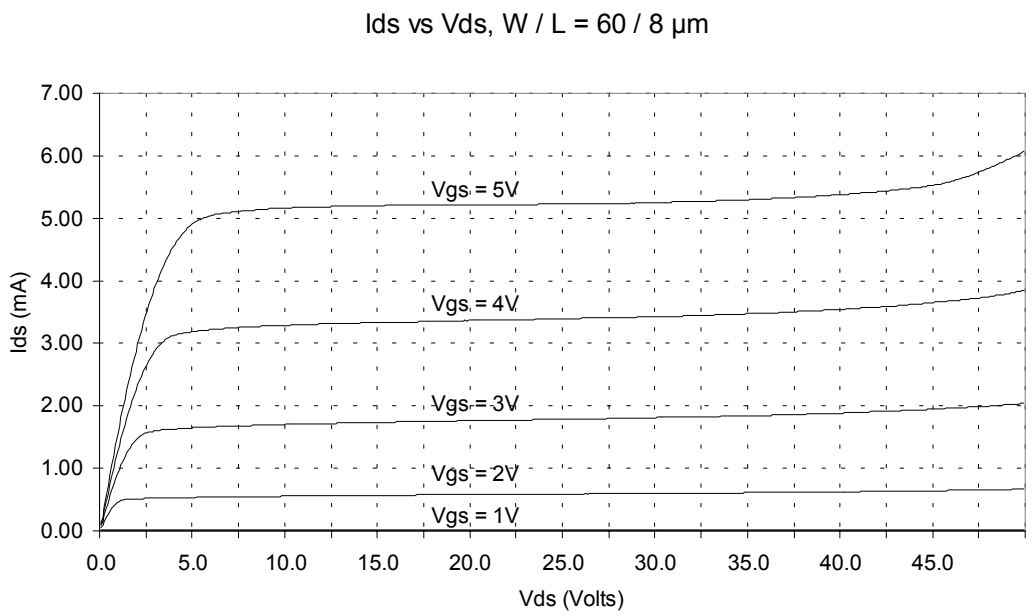


P-CH transistor IV characteristics of a 20/1.2 device. (VDS = 5V)

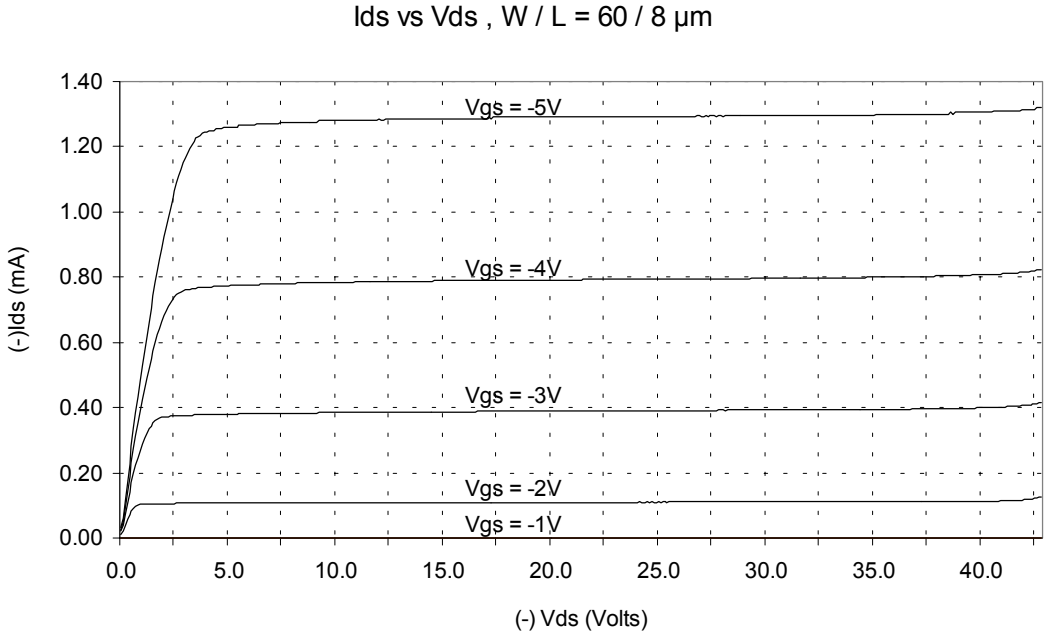


HV CMOS1.2 PROCESS

N-CH High Voltage transistor IV characteristics of a 60/8 device. (VDS = 35V)



P-CH High Voltage transistor IV characteristics of a 60/8 device. (VDS = 35V)



sames

HV CMOS1.2 PROCESS

ELECTRICAL CHARACTERISTICS

n-ch transistor (T = +25°C unless otherwise noted)

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.7	0.9	1.1	V	
Punch Through Voltage	$HVBVDSS_N$	40	45		V	
ON Resistance	$HVNR_{ON}$		500		Ω	@V_{GS} = 5V V_{DS} = 0.1V W/L = 60/8µm
Operating Voltage			V_{GS}=5V V_{DS}=35V		V	
N-Channel Low Voltage Transistor						
Threshold Voltage (linear extrapolated)	VTO_N	0.55	0.75	0.95	V	100/1.2 device
Body Factor	Y_N		0.35		$V^{½}$	100/1.2 device
Conduction factor (normalized)	β_N	64	75	86	$\mu A/V^2$	100/100 device
Effective Channel Length	$LEFF_N$	0.8	1.0	1.2	µm	100/1.2 device
Width Encroachment	ΔW_N		0.6		µm	per side
Punch Through Voltage	$BVDSS_N$	9			V	100/1.2 device
Poly Field Threshold	$VTF_{P(N)}$	10			V	
Threshold Voltage Offset (two sigmas)	ΔVTF_N		5		mV	100/10 device

HV CMOS1.2 PROCESS

p-ch transistor

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	0.7	0.9	1.1	V	
Punch Through Voltage	$HVBVDSS_P$	-38	-40		V	
ON Resistance	$HVPR_{ON}$		1800		Ω	@V_{GS} = -5V V_{DS} = -0.1V W/L = 60/8µm
Operating Voltage			V_{GS}=-5V V_{DS}=-35V		V	
P-Channel Low Voltage Transistor						
Threshold Voltage (linear extrapolated)	VTO_P	-1.1	-0.9	-0.7	V	100/1.2 device
Body Factor	Y_P		0.4		$V^{½}$	100/1.2 device
Conduction Factor (normalized)	β_P	20	25	30	$\mu A/V^2$	100/100 device
Effective Channel Length	$LEFF_P$	0.9	1.1	1.3	µm	100/1.2 device
Width Encroachment	ΔW_P		0.6		µm	per side
Punch Through Voltage	$BVDSS_P$			-8	V	100/1.2 device
Poly Field Threshold	$VTF_{P(P)}$			-10	V	
Threshold Voltage Offset (two sigmas)	ΔVTF_P		5		mV	100/10 device

HV CMOS1.2 PROCESS

diffusion & thin films

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Well (field) Sheet Resistance	$R_{W(+f)}$	0.7	1	1.2	kΩ/ []	n-well
N+ Sheet Resistance	R_{N+}	20	30	50	Ω/ []	
N+ Junction Depth	X_{JN+}		0.4		µm	
N-Well Junction Depth	x_{jnw}		0.3		µm	
P+ Sheet Resistance	R_{P+}	50	80	100	Ω/[]	
P+ Junction Depth	X_{JP+}		0.3		µm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	18	25	32	Ω/[]	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	15	25	50	Ω/[]	
Metal 1 Sheet Resistance (SLM)	R_{M1}		30		mΩ/ []	
Metal 1 Sheet Resistance (DLM)	R_{M2}		50		mΩ/ []	
Metal 2 Sheet Resistance (DLM)	R_{M2}		30		mΩ/ []	

capacitance

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Poly Gate to Bottom Poly	C_{PP}		0.86		$fF/\mu m^2$	interpoly capacitor
Metal 1 to Poly	C_{M1P}		0.057		$fF/\mu m^2$	
Metal 2 to Metal 1	C_{MM}		0.035		$fF/\mu m^2$	