



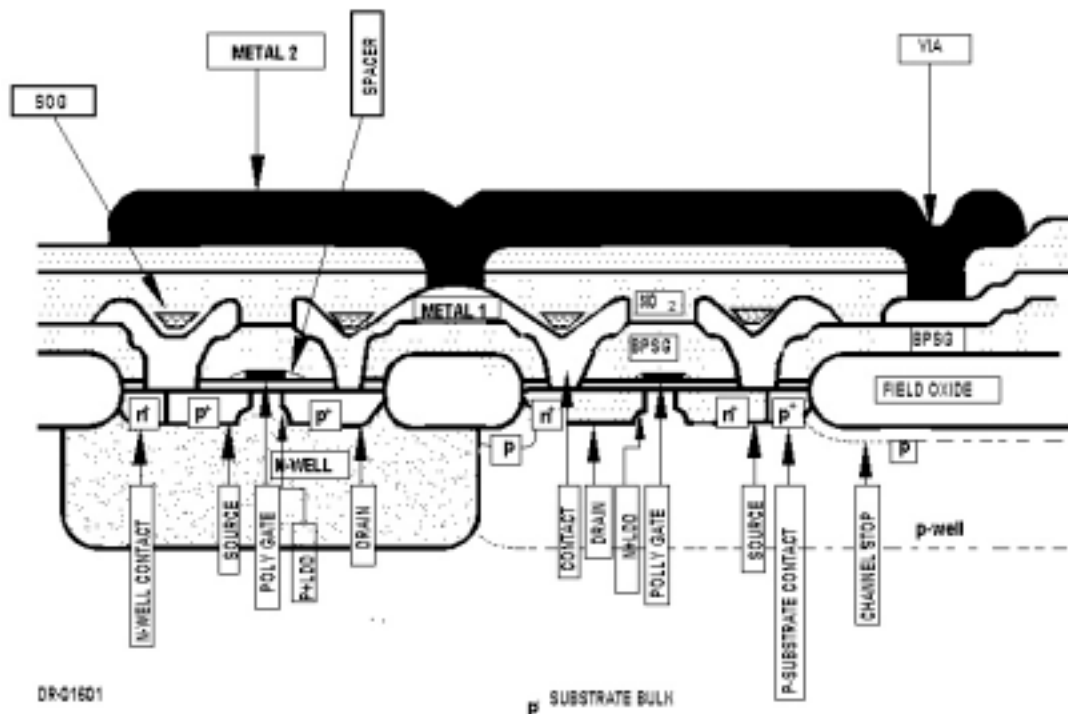
CMOS1.2 TWIN-WELL PROCESS

PHYSICAL CHARACTERISTICS

Process Geometry	1.2 micron
Process Number	C1233
Operating Voltage	5v
Well Doping	TWIN-WELL
Metal Layers	2
Poly Layers	1
Metal 1 Width	2.4 μm

Metal I Space	1.4 μm
Metall II Width	2.8 μm
Metal II Space	1.8 μm
Gate Poly Width	1.2 μm
Gate Poly Space	1.4 μm
N+ / P+ Space	0.8 μm
N+ to N-WELL	3.0 μm

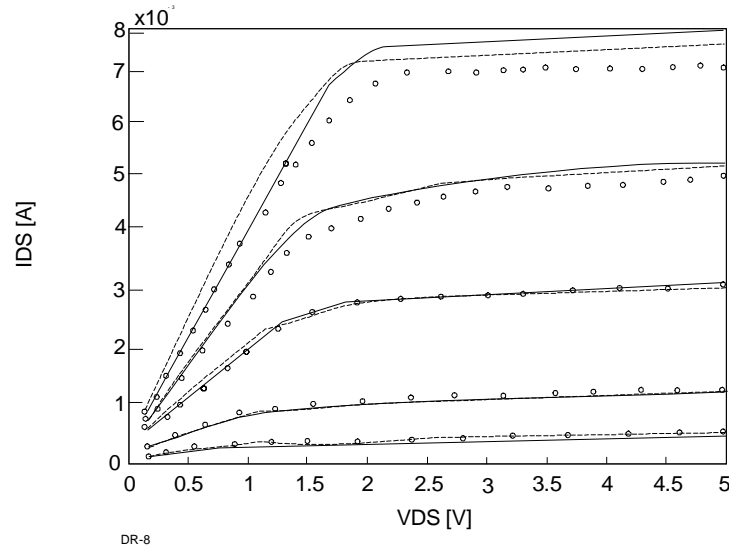
CROSS SECTIONAL VIEW OF THE CMOS 1.2 PROCES



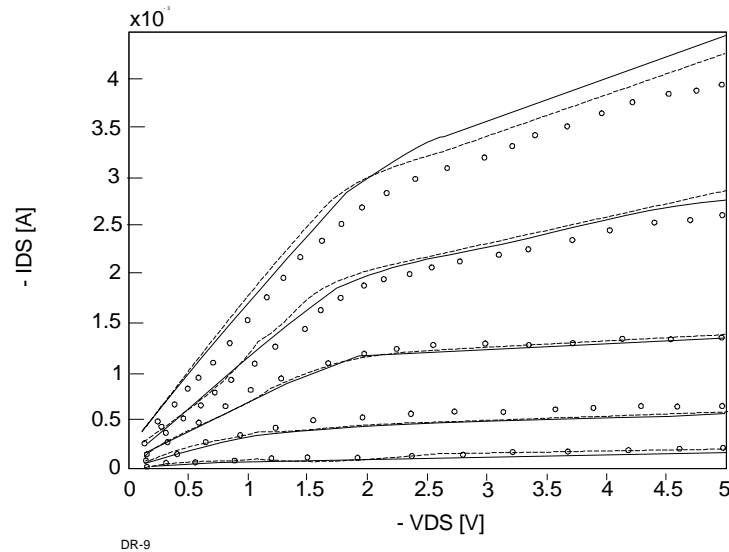


CMOS1.2 TWIN-WELL PROCESS

NMOS output characteristic of a typical wafer. $W/L=30/1.2$, $V_{GS}=1.5, 2, 3, 4, 5V$.
o=measured, solid line = MOS2 model, dashed line = ENG model.



PMOS output characteristic of a typical wafer. $W/L=30/1.2$, $-V_{GS}=1.5, 2, 3, 4, 5V$.
o=measured, solid line = MOS2 model, dashed line = ENG model.





CMOS1.2 TWIN-WELL PROCESS

ELECTRICAL CHARACTERISTICS

n-ch transistor

(T = +25°C unless otherwise noted)

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (Sat. extrapolated)	V_{TO_N}	0.57	0.71	0.82	V	30/1.2 device
Body Factor	V_N	0.6	0.74	0.78	$V^{1/2}$	30/30 device
Gain Factor	KPN	65	71.6	85	$\mu A/V^2$	3/30 device
Effective Channel Length	$LEFF_N$	0.9	1.1	1.03	μm	30/1.2 device
Width Encroachment	ΔW_N		0.4		μm	per side
Punch Through Voltage	$BVDSS_N$	10	14.7		V	30/1.2 device
Poly Field Threshold	$VTF_{P(N)}$	12	17.1		V	50/1.8 device

p-ch transistor

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (Sat. extrapolated)	V_{TO_P}	-0.86	-0.69	-0.61	V	30/1.2 device
Body Factor	V_P	0.43	0.50	0.57	$V^{1/2}$	30/30 device
Gain Factor	KPP	23	26.4	31	$\mu A/V^2$	30/30 device
Effective Channel Length	$LEFF_P$	0.9	1.1	1.3	μm	30/1.2 device
Width Encroachment	ΔW_P		0.45		μm	per side
Punch Through Voltage	$BVDSS_P$		-14	-8	V	30/1.2 device
Poly Field Threshold	$VTF_{P(P)}$		-15	-10	V	50/1.8 device

diffusion & thin films

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Well (field) Sheet Resistance	$T_{W(+f)}$	1.8	2.2	2.6	k Ω /	n-well
N-Well Junction Depth	x_{jnw}		3.5		μm	
N+ Sheet Resistance	R_{N+}	20	24	30	Ω /	
N+ Junction Depth	X_{JN+}		0.4		μm	
P+ Sheet Resistance	R_{P+}	25	46	55	Ω /	
P+ Junction Depth	X_{JP+}		0.4		μm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	22	27	30	Ω /	
Metal 1 Sheet Resistance (DLM)	R_{M1}		50		m Ω /	
Metal 2 Sheet Resistance (DLM)	R_{M2}		30		m Ω /	



CMOS1.2 TWIN-WELL PROCESS

capacitance

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Gate Oxide	C_{OX}	1.33	1.41	1.50	fF/ μm^2	
Metal 1 to Gate Poly (Area)	C_{M1P}	0.042	0.046	0.050	fF/ μm^2	
Metal 2 to Metal 1	C_{MM}		0.032		fF/ μm^2	