

CMOS1.2 Twin-Well Process

Electrical Characteristics

n-ch transistor

(T = +25°C unless otherwise noted)

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (Sat. extrapolated)	V_{TO_N}	0.57	0.71	0.087	V	30/1.2 device
Body Factor	γ_N	0.65	0.74	0.84	$V^{1/2}$	30/30 device
Gain Factor	KPN	63	71.6	85	$\mu A/V^2$	3/30 device
Effective Channel Length	L_{eff_N}	0.7	0.88	1.03	μm	30/1.2 device
Width Encroachment	ΔW_N		0.4		μm	per side
Punch Through Voltage	$BVDSS_N$	10	14.7		V	30/1.2 device
Poly Field Threshold	$VTF_{P(N)}$	12	17.1		V	50/1.8 device

p-ch transistor

Threshold Voltage (Sat. extrapolated)	V_{TO_P}	-0.9	-0.69	-056	V	30/1.2 device
Body Factor	γ_P	0.4	0.50	0.57	$V^{1/2}$	30/30 device
Gain Factor	KPP	22	26.4	32	$\mu A/V^2$	30/30 device
Effective Channel Length	L_{eff_P}	0.8	1.02	1.3	μm	30/1.2 device
Width Encroachment	ΔW_P		0.45		μm	per side
Punch Through Voltage	$BVDSS_P$		-14	-8	V	30/1.2 device
Poly Field Threshold	$VTF_{P(P)}$		-15	-10	V	50/1.8 device

diffusion & thin films

Well (field) Sheet Resistance	$T_{W(f)}$	1.8	2.2	2.6	$k\Omega/\square$	n-well
N-Well Junction Depth	X_{JNW}		3.5		μm	
N+ Sheet Resistance	R_{N+}	20	24	30	Ω/\square	
N+ Junction Depth	X_{JN+}		0.4		μm	
P+ Sheet Resistance	R_{P+}	33	46	53	Ω/\square	
P+ Junction Depth	X_{JP+}		0.4		μm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	20	27	35	Ω/\square	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	10	59	90	Ω/\square	
Top Poly Sheet Resistance	R_{POLYB}	23	31	38	Ω/\square	
Metal 1 Sheet Resistance (DLM)	R_{M1}		100		$m\Omega/\square$	
Metal 2 Sheet Resistance (DLM)	R_{M2}		70		$k\Omega/\square$	

capacitance

Gate Oxide	C_{OX}	1.38	1.44	1.65	$fF/\mu m^2$	
Poly Gate To Bottom Poly (Area)	C_{PP}	0.61	0.67	0.79	$fF/\mu m^2$	interpoly capacitor
Metal 1 to Gate Poly (Area)	C_{M1P}	0.049	0.053	0.058	$fF/\mu m^2$	
Metal 2 to Metal 1	C_{MM}		0.035		$fF/\mu m^2$	