

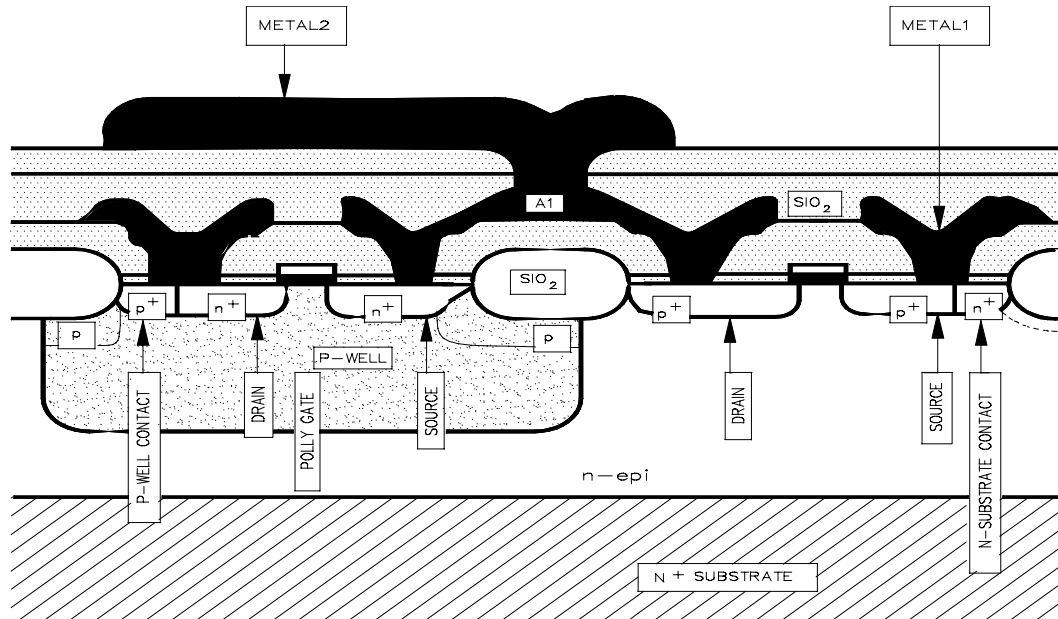


CMOS2 PROCESS

PHYSICAL CHARACTERISTICS

Process Geometry	2 micron
Process Number	C2001 (S.M) / C2005 (D.M)
Operating Voltage	5v
Well Doping	P-WELL
Metal Layers	2
Poly Layers	2
Contact	2 μ
Via	2 μ
Metal I Width	3.5 μ
Metal I Space	3.5 μ

Metal II Width	5.0 μ
Metal II Space	3.0 μ
Gate Poly Width	2.0 μ
Gate Poly Space	2.5 μ
Poly 2 Width	3.0 μ
Poly 2 Space	3.0 μ
N+/P+ Width	2.5 μ
N+/P+ Space	2.5 μ
N+ to P-WELL	7.0 μ
N+ to P+	9.5 μ



DR-00034

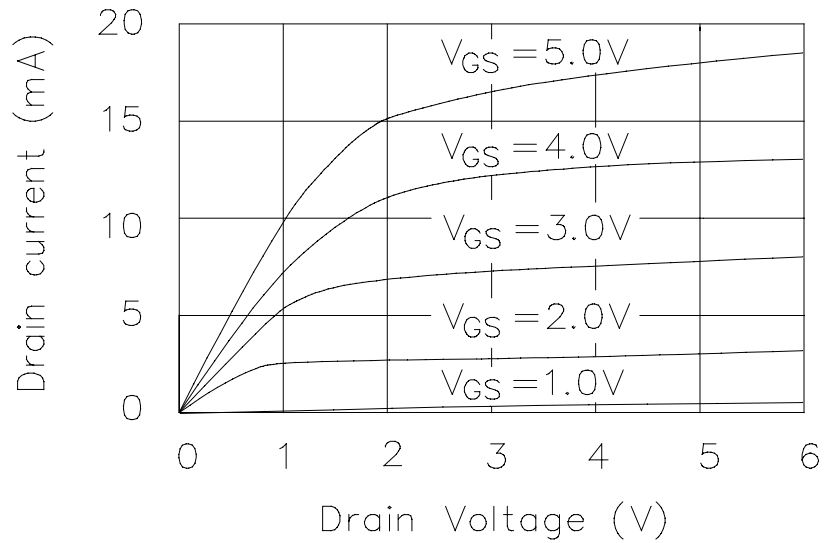
CROSS SECTIONAL VIEW OF THE CMOS 2 PROCESS



CMOS2 PROCESS

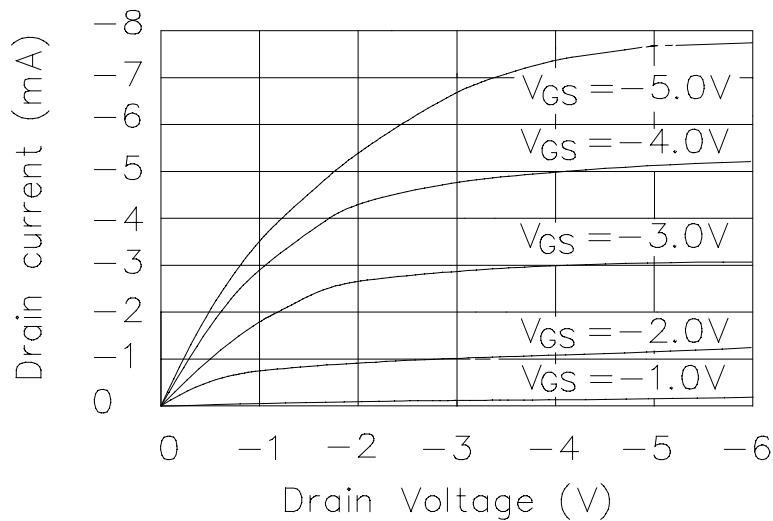
N-CH transistor IV characteristics of a 100/2.0 device

I_D vs V_D , $W/L = 100/2.0$



P-CH transistor IV characteristics of a 100/2.0 device

I_D vs V_D , $W/L = 100/2.0$





CMOS2 PROCESS

ELECTRICAL CHARACTERISTICS

n-ch transistor

(T = +25°C unless otherwise noted)

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	V_{TO_N}	0.4	0.7	0.8	V	100/2 device
Body Factor	γ_N		0.55		$V^{1/2}$	100/2 device
Conduction factor (normalized)	β_N	55	65	75	$\mu A/V^2$	100/100 device
Effective Channel Length	$LEFF_N$	1.2	1.5	1.9	μm	100/2 device
Width Encroachment	ΔW_N		0.6		μm	per side
Punch Through Voltage	$BVDSS_N$	10			V	100/2 device
Poly Field Threshold	$VTF_{P(N)}$	10			V	

p-ch transistor

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Threshold Voltage (linear extrapolated)	V_{TO_P}	-1.0	-0.8	-0.6	V	100/2 device
Body Factor	γ_P		0.45		$V^{1/2}$	100/2 device
Conduction Factor (normalized)	β_P	20	24	28	$\mu A/V^2$	100/100 device
Effective Channel Length	$LEFF_P$	1.1	1.35	1.7	μm	100/2 device
Width Encroachment	ΔW_P		0.8		μm	per side
Punch Through Voltage	$BVDSS_P$			-10	V	100/2 device
Poly Field Threshold	$VTF_{P(P)}$			-10	V	



CMOS2 PROCESS

diffusion & thin films

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Well (field) Sheet Resistance	$R_{W(+f)}$	1.4	2.5	43.2	k Ω /	p-well
N+ Sheet Resistance	R_{N+}	15	25	30	Ω /	
N+ Junction Depth	X_{JN+}		0.35		μm	
P+ Sheet Resistance	R_{P+}	60	75	100	Ω /	
P+ Junction Depth	X_{JP+}		0.35		μm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	10	22	30	Ω /	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	10	25	30	Ω /	
Bottom Poly Sheet Resistance	R_{POLYB}	10	22	30	Ω /	
Metal 1 Sheet Resistance (SLM)	R_{M1}		30		m Ω /	
Metal 1 Sheet Resistance (DLM)	R_{M2}		50		m Ω /	
Metal 2 Sheet Resistance (DLM)	R_{M2}		30		m Ω /	

capacitance

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Gate Oxide	C_{OX}	0.921	0.99	1.06	fF/ μm^2	
Poly Gate to Poly 2	C_{PP}	0.51	0.57	0.63	fF/ μm^2	interpoly capacitor
Metal 1 to Poly	C_{M1P}		0.049		fF/ μm^2	
Metal 2 to Metal 1	C_{MM}		0.035		fF/ μm^2	