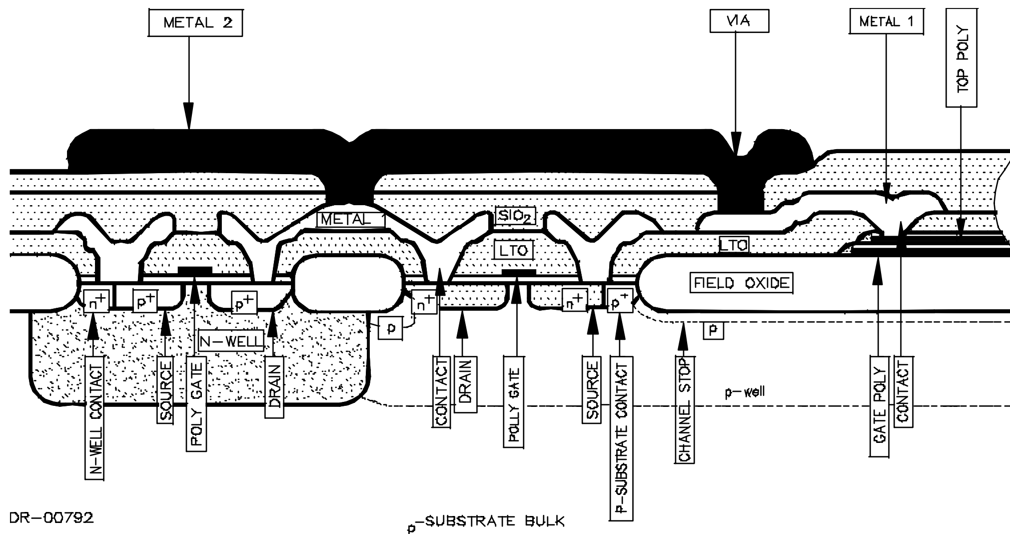
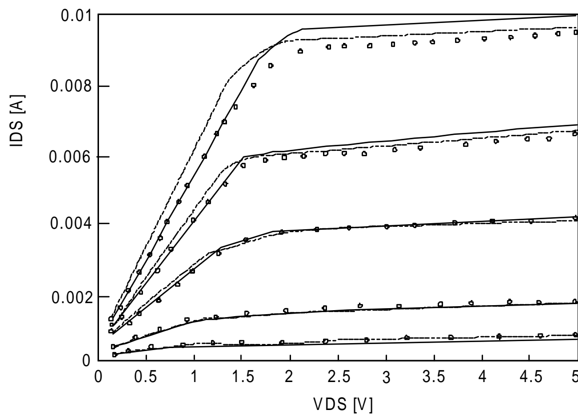
CMOS2.0 Twin-Well low Vth Process

Physical Characteristics

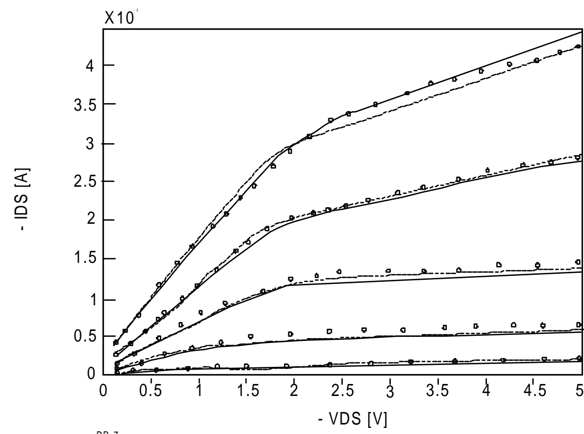
Process Geometry	2.0 Micron
Process Number	C2025
Operating Voltage	5v
Well Doping	Twin-WELL
Metal Layers	2
Poly Layers	2
Contact	2.0 x 2.0µm
Via	2.0 x 2.0µm
Metal I Width	3.0µm
Metal I Space	1.4µm
Metal II Width	3.0µm
Metal II Space	1.4µm
Gate Poly Width	2.0µm
Gate Poly Space	2.0µm
Top Poly Width	3.0µm
Top Poly Space	2.0µm
N+/P+Space	2.0µm
N+ to N-WELL	4.4µm
N+ to P+	8.8µm



CROSS SECTIONAL VIEW OF THE CMOS2.0 PROCESS



NMOS transfer characteristics of a typical wafer. W/L = 40/2, VGS = 1.5, 2, 3, 4, 5V. • = measured, solid line = MOS2 model, dashed line = AMS model.



PMOS transfer characteristics of a typical wafer. W/L = 40/2, -VGS = 1.5, 2, 3, 4, 5V. •= measured, solid line = MOS2 model, dashed line = AMS model.

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Electrical Characteristics

n-ch transistor (T = +25°C unless otherwise noted)

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (Sat. extrapolated)	VTO_N	0.4	0.53	0.65	V	40/2 device
Body Factor	γ_N	0.7	0.85	1.00	$V^{1/2}$	40/40 device
Gain factor	KPN	60	69	78	$\mu A/V^2$	40/40 device
Effective Channel Length	$Leff_N$	0.85	1.15	1.45	µm	40/2 device
Width Encroachment	ΔW_N		0.6		µm	per side
Punch Through Voltage	$BVDSS_N$	10	15		V	40/2 device
Poly Field Threshold	$VTF_{P(N)}$	10	17		V	50/2 device

p-ch transistor

Parameters	Sym	Min	Typ	Max	Unit	Comments
Threshold Voltage (Sat. extrapolated)	VTO_P	-0.55	-0.65	-0.75	V	40/2 device
Body Factor	γ_P	0.48	0.55	0.62	$V^{1/2}$	40/40 device
Gain Factor	KPP	20	24	28	$\mu A/V^2$	40/40 device
Effective Channel Length	$Leff_P$	1.05	1.35	1.65	µm	40/2 device
Width Encroachment	ΔW_P		0.6		µm	per side
Punch Through Voltage	$BVDSS_P$		-14	-10	V	40/2 device
Poly Field Threshold	$VTF_{P(P)}$		-15	-10	V	

diffusion & thin films

Parameters	Sym	Min	Typ	Max	Unit	Comments
Well (field) Sheet Resistance	$T_{W(+f)}$	1.8	2.2	2.6	kΩ/☐	n-well
N-Well Junction Depth	X_{JNW}		3.5		µm	
N+ Sheet Resistance	R_{N+}	20	30	40	Ω/☐	
N+ Junction Depth	X_{jN+}		0.5		µm	
P+ Sheet Resistance	R_{P+}	45	70	100	Ω/☐	
P+ Junction Depth	X_{jP+}		0.55		µm	
Gate Poly Sheet Resistance (n-ch)	R_{POLYN}	13	17	21	Ω/☐	
Gate Poly Sheet Resistance (p-ch)	R_{POLYP}	14	22	30	Ω/☐	
Top Poly Sheet Resistance	R_{POLYB}	20	48	75	Ω/☐	
Metal 1 Sheet Resistance (DLM)	R_{M1}		100		mΩ/☐	
Metal 2 Sheet Resistance (DLM)	R_{M2}		70		kΩ/☐	

capacitance

Parameters	Sym	Min	Typ	Max	Unit	Comments
Gate Oxide	C_{OX}	1.05	1.11	1.19	$fF/\mu m^2$	
Poly Gate To Bottom Poly (Area)	C_{PP}	0.41	0.45	0.49	$fF/\mu m^2$	interpoly capacitor
Metal 1 to Gate Poly (Area)	C_{M1P}	0.043	0.049	0.058	$fF/\mu m^2$	
Metal 2 to Metal 1	C_{MM}		0.05		$fF/\mu m^2$	