# RM4301ASEA Application Note:
# Low-Cost Three-Phase Watt-Hour Energy Meter

## RM4301ASEA

## FEATURES

- Designed to exceed IEC62053-21 requirements for class 1 active energy meters
- Selectable rated conditions, LED pulse rates and counter resolutions
- On-board precision calibration
- Direct drive capability for stepper motor or impulse counter
- Opto-isolated output for connection to measurement equipment
- Per phase mains voltage and energy direction indicator LEDs

## INTRODUCTION

This application note addresses various design aspects of a low-cost three-phase watt-hour energy meter based on the SAMES SA4301A integrated circuit. The SA4301A is a single-chip solution for accurate bi-directional three-phase energy measurement. It incorporates an on-chip oscillator and has a direct drive capability for a stepper motor or an impulse counter. The emphasis for the design of this meter has been placed on exceeding the specifications whilst incurring the lowest possible cost. The specification for this design is the International Standards IEC62053-21. This meter is designed to meet all class 1 sections of the IEC62053-21 specification that relate to electrical characteristics.

## METER SPECIFICATIONS

A basic meter block diagram using the SA4301A is shown in Figure 1. The three load currents are sensed with current transformers and converted to the required input currents via the current input networks. The scaled mains voltage signals are applied to the SA4301A via three voltage divider circuits. Calibration is done by means of a resistive network on these voltage sensing networks. Both the current and voltage input networks incorporate low-pass filters to improve the meters performance, especially the immunity to electromagnetic disturbances. The measured energy is displayed on a stepper motor or an impulse counter. An LED as well as an optical isolator provide an electrically isolated connection to measurement equipment during calibration and performance verification.

The most important IEC62053-21 class 1 accuracy specifications to which the meter was designed are listed in Table 1 on page 2. The typical value of $I_{MAX}$ is 4x to 10x Ib.

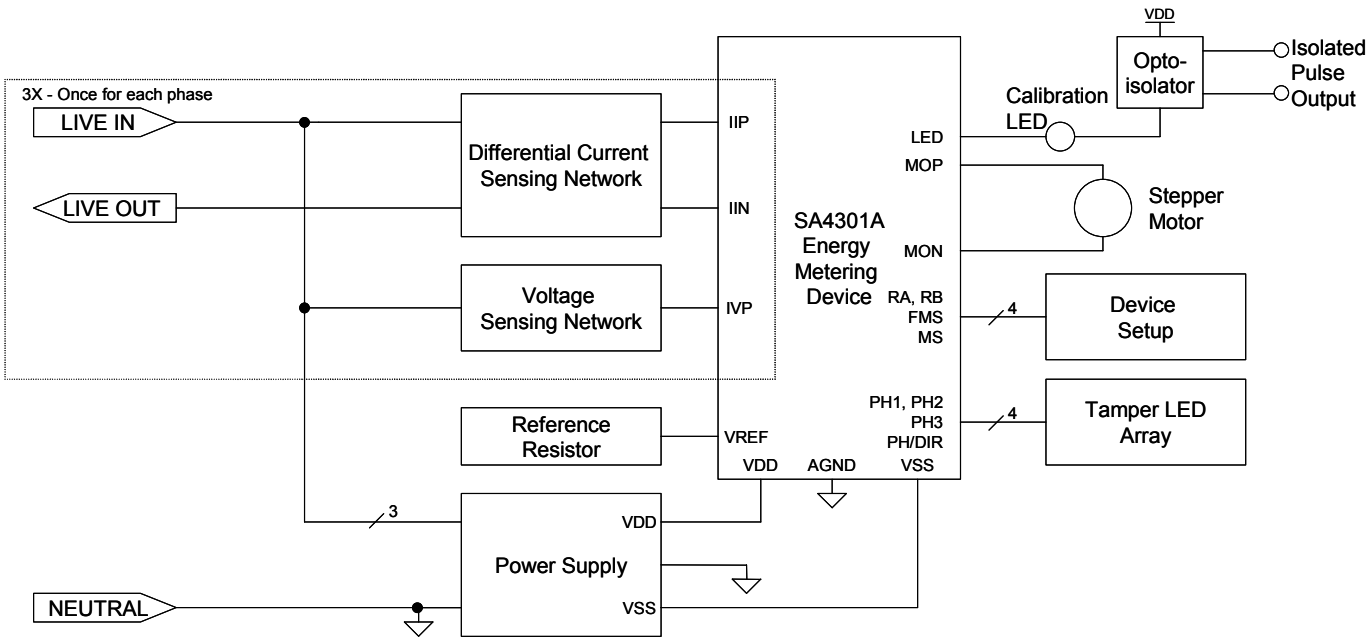


*Figure 1: Block diagram of a three-phase watt-hour meter based on the SA4301A*

| Current Value | Load | Power Factor | Class 1 Error Limits |
|---|---|---|---|
| $0.05Ib \leq I < 0.1Ib$ | Balanced three phase | 1 | ± 1.5% |
| $0.1Ib \leq I \leq I_{MAX}$ | Balanced three phase | 1 | ± 1.0% |
| $0.1Ib \leq I < 0.2Ib$ | Balanced three phase | 0.5 inductive (lag) | ± 1.5% |
| $0.1Ib \leq I < 0.2Ib$ | Balanced three phase | 0.8 capacitive (lead) | ± 1.5% |
| $0.2Ib \leq I \leq I_{MAX}$ | Balanced three phase | 0.5 inductive (lag) | ± 1.0% |
| $0.2Ib \leq I \leq I_{MAX}$ | Balanced three phase | 0.8 capacitive (lead) | ± 1.0% |
| $0.1Ib \leq I \leq I_{MAX}$ | Single phase | 1 | ± 2.0% |
| $0.2Ib \leq I \leq I_{MAX}$ | Single phase | 0.5 inductive (lag) | ± 2.0% |

*Table 1: IEC62053-21 Accuracy Specifications*

# CIRCUIT DESIGN PRINCIPLES

## CURRENT SENSING NETWORKS

The primary function of the current sensing networks is to sense the load currents and convert them to the input current signals required by the SA4301A. The current sensing network for one phase is shown in Figure 2. The sensing networks for all phases are identical.

The amplitude of the input current into the SA4301A at maximum current ($I_{MAX}$) should be set as close as possible to $16\mu A_{RMS}$. The current input of the device saturates at 25µA peak current, so the $16\mu A_{RMS}$ input current (22.62µA peak) allows for an over-current up to 110% $I_{MAX}$ before saturation occurs. The SA4301A can be used with most available current transformers.

The burden resistor of the current transformer should be selected such that the voltage across the resistor at maximum current ($I_{MAX}$) is in the order of $100mV_{RMS}$. It is best that this voltage does not exceed $200mV_{RMS}$. The reference level should be connected in the centre of the burden resistor to create purely differential current inputs. This will result in the best linearity for the meter. Resistors RX14 and RX15 form the burden resistor. The best value of each burden resistor is determined by using

$$RX14 = RX15 = \frac{100mV \times N_{CT}}{2 \times I_{MAX}} = R_B \quad (1)$$

to calculate the theoretical value of the burden resistor and then rounding this up to the nearest available resistor value. $N_{CT}$ is the turns ratio of the current transformer.

The internal current feedback present on the differential current inputs IIN and IIP of the SA4301A creates a virtual short circuit between the two current input pins. This means that the resistor value required to generate the correct input current can be calculated using:

$$RX16 = RX17 = RX18 = RX19 = \frac{I_{MAX} \times 2 \times R_B}{N_{CT} \times 16 \times 10^{-6}} \times \frac{1}{4} = R_C \quad (2)$$

where $R_B$ is the actual value of the burden resistor used.

A secondary function of the current sense networks is to attenuate all high frequency components that could disrupt the accuracy of the SA4301A. These high frequency components may occur due to high frequency surges (fast transient burst), may be induced through strong electric fields or may simply be noise on the power lines. Certain high frequency components, typically those close to integer multiples of the sampling frequency of the analog to digital converters will be mapped close to 50Hz once sampled (a process known as aliasing) and will distort the accuracy of the converters. This can be prevented by adequately attenuating all high frequency signal components. The typical oscillator frequency is 3.58MHz and the analog to digital converters of the SA4301A operate at one half of this frequency, so the filters should be designed to give sufficient attenuation at 1.79MHz. This can readily be achieved by placing a single order RC low pass filter on each current input as shown in Figure 2. The capacitors cannot be placed directly on the input pins IIN and IIP because no differential voltage signal exists between these pins due to the virtual short circuit created by the input network of the SA4301A. The input resistance is therefore split into two equal resistors (RX16/RX17 and RX18/RX19) and the capacitor is placed between these resistors. Now a differential voltage can appear across the capacitors and hence filter high frequencies. The lowest -3dB cut-off frequency (and hence best filtering ability) for a given capacitor value is achieved when all four input resistors are equal (RX16 = RX17 = RX18 = RX19 = $R_C$). The current input networks must be balanced so both capacitors must also be equal (CX2 = CX3 = $C_C$). In this case the equivalent resistance associated with each capacitor is ½$R_C$ and the -3dB cut-off frequency is:

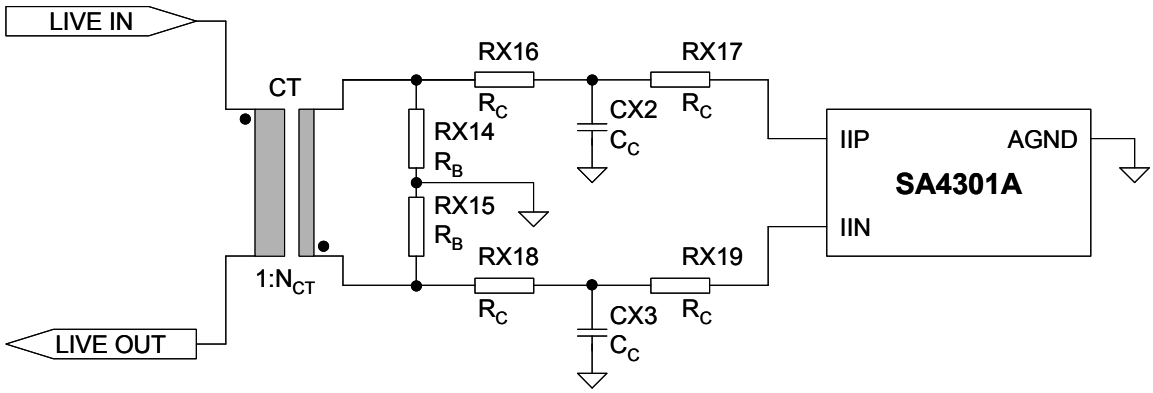


*Figure 2: Circuit diagram of one current sensing network*

$$f_{CI,-3dB} = \frac{1}{\pi R_C C_C} \quad (3)$$

This frequency should be somewhere between 10kHz and 20kHz to ensure both adequate attenuation at integer multiples of the analog to digital converters sampling frequency, and very low phase shift and gain error at mains frequency and its relevant harmonics. The requirement for the very low phase shift is explained under the "Voltage Sense Networks" section.

## VOLTAGE SENSING NETWORK

The voltage sensing networks perform similar functions to the current sensing networks. They sense the mains voltages and convert them to the input current signals required by the SA4301A, as well as compensating for the phase shift of the current transformers used on the current sensing networks. They also filter all unwanted signals and thereby ensure that the performance of the SA4301A is not affected. The voltage sensing network for one phase is shown in Figure 3. The sensing networks for all phases are identical.

The voltage sensing network is composed of an adjustable voltage divider (resistors RX0 to RX12) and the current input resistor RX13 that generates the required current input signal for the SA4301A. The first consideration when designing the voltage sensing network is that the -3dB cut-off frequency has to be accurately related to that of the current sensing network. This is important to ensure that the phase shift experienced by the voltage and current signals is identical. If this is not the case the energy meter will have poor performance under non-unity power factor conditions. The high cut-off frequency of the input network filters does ensure that this matching does not have to be extremely precise. This allows component tolerances to be accommodated without seriously affecting the performance of the meter. The best matching conditions between the cut-off frequencies is achieved by using identical capacitors on both the current and voltage sensing networks, so CX1 should equal CX2 and CX3. The IVP input is a virtual short circuit to analog ground (AGND) so the equivalent resistance associated with CX1 is

$$R_{equ-CX1} = RX12 \,||\, RX13 \,||\, R_X \quad (4)$$

where $R_X$ is the series combination of RX0, RX1, RX2 and $R_{trim}$. Further, $R_{trim}$ is the series combination of the resistors RX3 to RX11 that can be enabled or disabled to calibrate the meter. If both $R_X$ and RX13 are designed to be significantly larger than RX12 then

$$R_{equ-CX1} \approx RX12\,. \quad (5)$$

The overall phase shift of the current sensing networks and the voltage sensing networks needs to be matched to ensure that the performance of the meter at non-unity power factors will not be affected. This is done by purposefully increasing the -3dB cut-off frequency of the anti-alias filters on the voltage input networks.

The phase shift of the current input network is

$$\phi_{II} = -\arctan(\pi R_C C_C \times f_{Mains})\,. \quad (6)$$

Additionally it is given that the phase shift of the voltage input network has to be

$$\phi_{IV} = \phi_{II} + \phi_{CT}\,, \quad (7)$$

where $\phi_{CT}$ is the phase shift of the current transformer. Assuming the result of equation (5) the value of RX12 can be calculated as

$$RX12 = \frac{|\tan\phi_{IV}|}{2\pi C_C \times f_{Mains}}\,, \quad (8)$$

and the resulting -3dB cut-off frequency of the voltage network anti-alias filter is

$$f_{CV,-3dB} = \frac{1}{2\pi \times RX12 \times C_C} . \quad (9)$$

The value of the cut-off frequency of the voltage input network is less critical than that of the current input network because the dynamic range required on the voltage input network is small. A cut-off frequency between 10kHz and 25kHz is acceptable.

The voltage input IVP of the SA4301A has to be driven with a current of $11\mu A_{RMS}$ at the nominal rated mains voltage of 220V. This input also saturates at 25µA peak current, so the $11\mu A_{RMS}$ input current allows for 50% overdrive capability while maintaining linearity. This ensures that the device will not saturate with a ±20% variation in mains voltage. The simplest method is to set the input resistor RX13 at 100 times the value of RX12, thereby satisfying the condition for equation (5). This choice sets the required output voltage on the voltage divider to

$$V_D = 11 \times 10^{-6} \times 100 \times RX12 \quad (10)$$

because the IVP pin has a virtual short to ground. Given that RX13 and $R_X$ are large compared to RX12

$$V_D = \frac{RX12}{RX12 + R_X} \times V_{NOM} \approx \frac{RX12}{R_X} \times V_{NOM} \quad (11)$$

Combining these equations results in

$$R_X = \frac{V_{NOM}}{11 \times 10^{-4}} \approx 909\ V_{NOM} , \quad (12)$$

which should easily satisfy the condition that $R_X$ should be significantly larger than RX12. It must be noted that $R_X$ changes during calibration of the meter, so if the stated condition is not met, the -3dB cut-off frequency of the voltage sensing network will change during calibration of the meter which is not desirable.

A calibration mechanism is required to compensate for component tolerances. The SA4301A is the component that will exhibit the widest tolerance and has a gain variation of ±10%. All resistors should be 1% metal film resistors so that the resistor tolerance will not add significant overall deviation. The total tuning range can therefore be designed as ±15%. A binary weighted series combination of nine resistors will then allow calibration to an accuracy of 30%/512 = 0.06% which is considered sufficient for a low-cost class 1 energy meter. To achieve approximately 15% tuning range in either direction around the nominal point the highest resistance in the calibration network (RX3) should be 15% of $R_X$ with each subsequent resistor having half the value of the previous one. The values of the voltage divider and calibration network are then designed using

$$RX0 + RX1 + RX2 = R_X - 15\%R_X = 0.85R_X , \quad (13)$$
$$RX3 = 15\%R_X , \quad (14)$$
$$RX4 = 0.5 \times RX3,\ RX5 = 0.5 \times RX4, \text{ etc.} \quad (15)$$

This topology of current and voltage input networks has some advantages for mass production. The first is that the value of $R_X$ which is used to determine the calibration network is independent of RX12. This is important because the value of RX12 is related to that of the current input resistors (RX16 to RX19) which will be specific to the current transformer. The CT can therefore be changed without having to adapt the calibration network, i.e. the calibration network is universal. Secondly, the value of RX12 can be changed to adapt the phase compensation without affecting the calibration network. Any change in RX12 is the simply reflected in RX13 and the input networks are guaranteed to be correct.

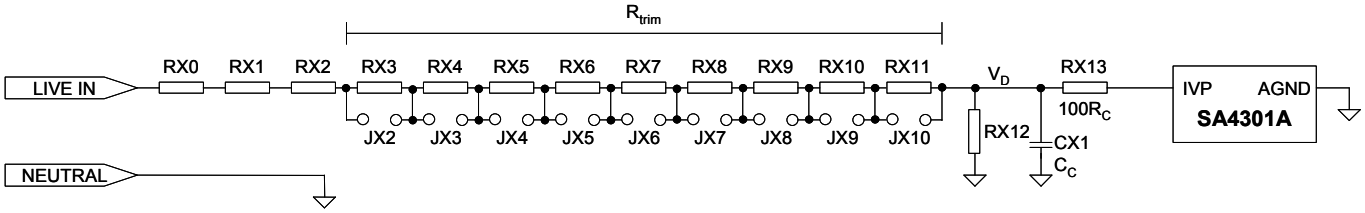


*Figure 3: Circuit diagram of one voltage sensing network*

## SA4301A RELATED CIRCUITRY

All aspects discussed in this section are illustrated on the complete meter schematic (Figure 7). The SA4301A requires a split supply of +2.5V (VDD) and -2.5V (VSS) around the meter ground node, which has to be connected to the AGND pin of the SA4301A. These three supply lines have to be properly decoupled using capacitors C10 and C11 (220nF ceramic each) between the supplies and ground and C12 (1µF ceramic) between the two supplies. These capacitors are required to achieve good performance and have to be placed as close to the device as possible. Their placement is as important as their presence, placing them more than a few millimeters away from the device renders them useless. The on-chip reference current is derived from a 47kΩ resistor (R3) connected between VREF and VSS. This resistor must be a 1% tolerance metal film type or similar. The metal film ensures that less noise will be induced into the device pin. This reference resistor should be placed as close as possible to the device and C11.

The internal pulse dividers of the SA4301A are configured through the pins RA, RB and FMS. These pins must either be tied to VDD, VSS, PH/DIR or left floating. The FMS pin cannot be tied to PH/DIR and will enable a fast pulse output mode when left floating, which is typically not applicable to an energy meter of this type. The setup pins should be directly connected to VDD, VSS or PH/DIR, no pull-up or pull-down resistors are required.

The stepper motor used to display the consumed energy should be connected to the MOP and MON pins through two small current limiting resistors (R8 and R9). For calibration and performance verification purposes an LED and opto-isolator are connected in series to the LED output pin of the SA4301A. This output is active low so the LED and opto-isolator are connected through a current limiting resistor to VDD.

For more elaborate information on setting up and using the SA4301A, refer to the SA4301A datasheet available on the SAMES website at www.sames.co.za or from any SAMES representative.

## SETUP OF RA, RB AND FMS FOR RATED CONDITIONS

The following equations and table state the basic pulse constants and motor constants obtainable with the SA4301A.

The pulse rate of the LED output for a balanced 3 phase load is:

$$p/kWh_{LED} = \frac{IVP}{16} \times 5000 \times \frac{1}{DF\_LED} \times \frac{3600 \times 1000}{3 \times V_{NOM} \times I_{MAX}} \qquad (16)$$

where IVP is the input current to the SA4301A at $V_{NOM}$ and assuming that the input current at $I_{MAX}$ on the current inputs is $16\mu A_{RMS}$. For $V_{NOM}$ = 220V the IVP input current should typically be 11µA.

The motor output pulse rate is

$$p/kWh_{MOTOR} = p/kWh_{LED} \times \frac{1}{DF\_MO} \qquad (17)$$

The variables DF_LED and DF_MO are defined by setting FMS, RA and RB according to Table 2.

| FMS | RB | RA | DF_LED | DF_MO |
|---|---|---|---|---|
| 0 | 0 | 0 | 146 | 128 |
| 0 | 0 | 1 | 292 | 64 |
| 0 | 0 | Z | 584 | 32 |
| 0 | 0 | PH/DIR | 1168 | 16 |
| 0 | 1 | 0 | 146 | 64 |
| 0 | 1 | 1 | 292 | 32 |
| 0 | 1 | Z | 584 | 16 |
| 0 | 1 | PH/DIR | 1168 | 8 |
| 0 | Z | 0 | 146 | 32 |
| 0 | Z | 1 | 292 | 16 |
| 0 | Z | Z | 584 | 8 |
| 0 | Z | PH/DIR | 1168 | 4 |
| 0 | PH/DIR | 0 | 146 | 16 |
| 0 | PH/DIR | 1 | 292 | 8 |
| 0 | PH/DIR | Z | 584 | 4 |
| 0 | PH/DIR | PH/DIR | 1168 | 2 |
| 1 | 0 | 0 | 976 | 32 |
| 1 | 0 | 1 | 1952 | 16 |
| 1 | 0 | Z | 234 | 32 |
| 1 | 0 | PH/DIR | 468 | 16 |
| 1 | 1 | 0 | 392 | 16 |
| 1 | 1 | 1 | 784 | 8 |
| 1 | 1 | Z | 234 | 16 |
| 1 | 1 | PH/DIR | 468 | 8 |
| 1 | Z | 0 | 392 | 8 |
| 1 | Z | 1 | 784 | 4 |
| 1 | Z | Z | 234 | 8 |
| 1 | Z | PH/DIR | 468 | 4 |
| 1 | PH/DIR | 0 | 196 | 8 |
| 1 | PH/DIR | 1 | 392 | 4 |
| 1 | PH/DIR | Z | 156 | 8 |
| 1 | PH/DIR | PH/DIR | 312 | 4 |

*Table 2: Division factors available on the SA4301A*

*'0' indicates that the input is connected to VSS*
*'1' indicates that the input is connected to VDD*
*'Z' indicates that the input is left floating*
*'PH/DIR' indicates that the input is connected to PH/DIR*

## POWER SUPPLY

The RM4301ASEA meter uses a transformer based supply with a single 7805 regulator to generate a stable 5V supply. This supply is then split into two 2.5V supplies by means of a resistive divider. The center of this divider is connected to the reference level of the meter to create the required +2.5V and -2.5V power supply for the SA4301A. The complete power supply circuit is shown in Figure 4. Due to the use of transformers this supply can still operate the circuit when two phases are missing and the mains voltage drops to below $0.8V_{NOM}$. Additionally it conforms to the power requirements of the IEC specification, even when the mains voltage increases to beyond $1.2V_{NOM}$.

## TAMPER INDICATORS

The SA4301A has built in tamper indication features that use six LEDs to display the mains voltage failure as well as reverse energy on a per phase basis. The RM4301ASEA contains the standard LED tamper array in order to display these tamper conditions as shown in Figure 5. If a specific mains voltage LED is off this means that that mains voltage has failed. Reverse energy is indicated by a specific direction LED turning on. Should all three mains voltage LEDs flash, a phase sequence error is present.

## IMMUNITY TO ELECTROMAGNETIC DISTURBANCE

The typical electromagnetic disturbances that can cause the meter to fail or incorrectly record energy are:

- Electrostatic discharge and surges
- Electromagnetic HF (high frequency) fields
- Fast transient burst (FTB)

Typically these disturbances will either cause complete and permanent failure by damaging the sensitive CMOS circuitry of the SA4301A through high voltage levels or cause incorrect registration of energy through high frequency signals that are aliased into the operating bandwidth of the device, thereby disrupting the energy calculation algorithm. The immunity of a class 1 watt-hour meter to these types of disturbances is prescribed by the IEC62053-21 specification.

Generally two protection mechanisms are required. The first is to ensure that dangerously high voltage levels are sufficiently attenuated or clamped so that no permanent damage can occur to the SA4301A and other sensitive

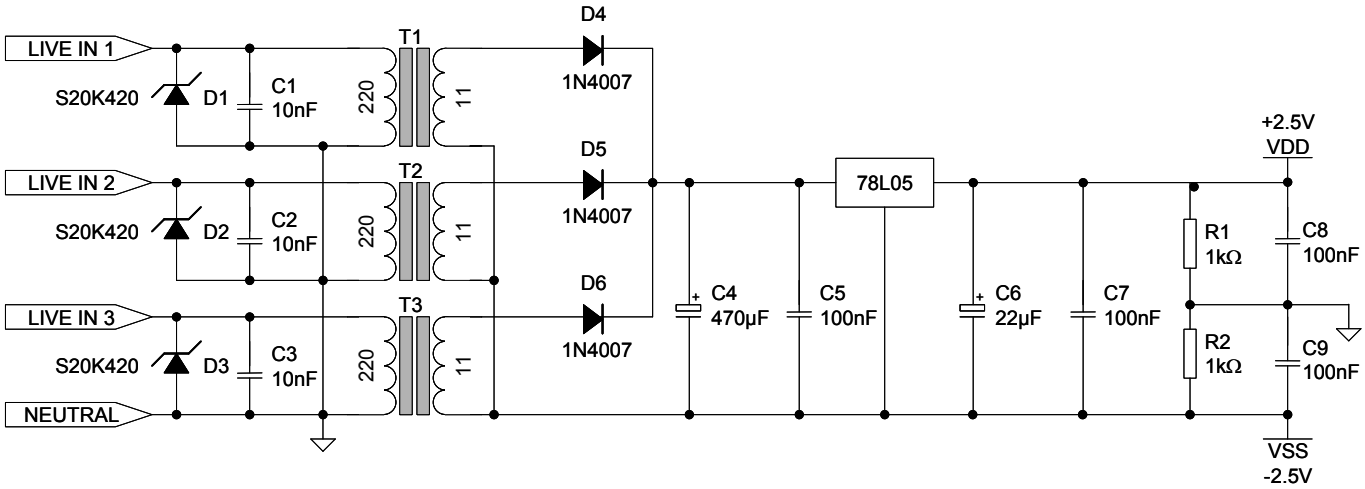


*Figure 4: Circuit diagram of the power supply circuit*

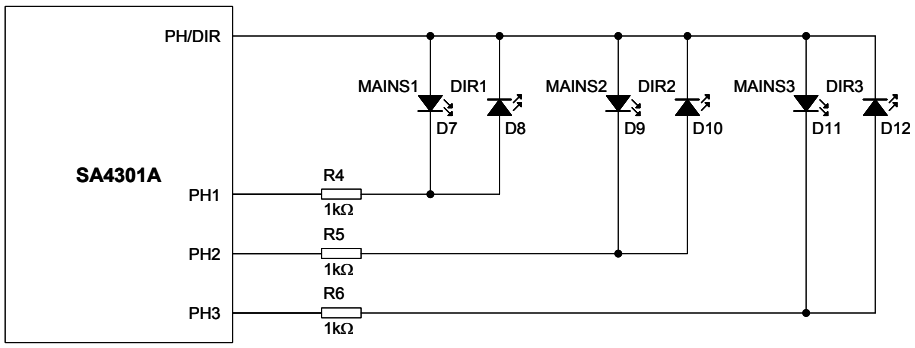


*Figure 5: Tamper LED array*

components. To ensure this the complete meter is protected with an S20K420 MOV (Metal Oxide Varistor) from each phase to neutral to clamp any high voltage potentials . A 10nF capacitor is placed in parallel with each MOV to ensure that any parasitic inductance that can increase the amplitude and duration of dangerous voltage spikes, is cancelled. Each LIVE IN and NEUTRAL input is connected directly across an MOV with the lowest possible impedance. With the MOV and the protection capacitor in place all extremely high voltage levels are clamped. Typically a larger MOV can absorb more energy and will therefore be more effective at clamping high voltage levels to protect the SA4301A. The subsequent filtering and attenuation of the input networks will also ensure that no damage can occur to the SA4301A by further reducing the voltage levels that can reach the device.

An MOV alone will not be sufficient to ensure that the meters performance is not affected by the presence of electromagnetic disturbances during operation. All high frequency signal components need adequate filtering by the filters in the current sensing networks, voltage sensing networks and the power supply. This should ensure that the meters performance is not affected by the presence of high frequency signals that are directly applied (FTB test) or induced (HF immunity test). The immunity to these types of interference can be improved by reducing the cut-off frequency of the filter networks. This is however only practical to a certain point, before poor matching between the filters on the voltage and current channels causes linearity issues at non-unity power factor. Alternatively ferrite beads could be used to enhance the filtering, by using them between the SA4301A and the power supply on the VDD, VSS and GND lines. This is however seldom necessary.

## PCB DESIGN CONSIDERATIONS

There are numerous PCB design aspects to consider when designing an energy meter using the SA4301A. These principles have all been incorporated in the sample PCB layout given in the “PCB Layout” section.

The first is the location of critical components. The current and voltage sensing input resistors (RX13 and RX16 to RX19) with their associated low pass filtering capacitors (CX1 to CX3) should be located as close to the device pins as possible. The same holds for the reference resistor (R3) and the supply bypass capacitors (C10 to C12). All these resistors should be 1% metal film resistors.

Special care is required as far as the current transformer burden resistors are concerned. Very often the low ohmic resistors have poor temperature coefficient which will affect the performance of the meter. It has been found that standard leaded resistors are more suitable for the burden resistors than the surface mount equivalents.

The SA4301A should be placed on a solid ground plane that is connected to the AGND pin of the device. This ground plane should be kept clear of noise by only connecting it to the ground plane of the power supply and the NEUTRAL input at a single point. It should also be kept away from any high frequency, high voltage or high current signals that may induce noise. For example, the first section of the voltage input attenuation network (RX0 to RX2) should be placed far away from this ground plane. If a ferrite bead is used to connect the rest of the meters ground to this ground plane then identical ferrite beads must be placed into the power supply lines (VDD and VSS) If only a single ferrite bead is placed some signals are filtered and others are not, which will create differential noise between the unfiltered and the filtered signals. This will affect the performance of the SA4301A in the presence of electromagnetic disturbance.

As far as the immunity to electromagnetic interference is concerned the guideline is simply to minimize the parasitic inductance. Each PCB net has a parasitic inductance and if this is not sufficiently small it could cause resonance with the parasitic capacitance at low enough frequencies to affect the performance on the HF interference test or the FTB test. Keeping the PCB tracks as short as possible is one method to avoid this scenario. Parasitic inductance is also a factor that can render the MOV almost useless because a voltage spike can be amplified in both magnitude and duration by series inductance. The capacitor in parallel with the MOV cancels some of this inductance but still all possible measures to avoid parasitic inductance should be adhered to.

## DETAIL DESIGN

The detailed specifications are:
Nominal voltage: $V_{NOM}$ = 220V
Maximum current: $I_{MAX}$ = 60A
Basic current: Ib = 10A
Mains frequency: $f_{Mains}$ = 50Hz
CT: $N_{CT}$ = 1000, $\phi_{CT}$ = 0.09º
Pulse constant: 800imp/kWh
Motor constant: 100imp/kWh

Using the design equations derived earlier:
equation(1): $R_B$ = 0.83Ω ≈ 1.2Ω (readily available)
equation(2): $R_C$ ≈ 2.2kΩ
equation(3): Target $f_{CI,-3dB}$ = 10kHz for best immunity and so $C_C$ ≈ 15nF
equation(6): $\phi_{II}$ = -0.297º
equation(7): $\phi_{IV}$ = -0.207º

equation(8): RX12 ≈ 750Ω

equation(9): $f_{CI,-3dB} \approx 14.1kHz$ (acceptable)
equation(12): $R_X = 200k\Omega$
equation(13): choose RX0 = RX1 = 62kΩ and obtain RX2 ≈ 47kΩ
equation(14): RX3 = 30kΩ
equation(15): RX4 = 15kΩ, RX5 = 7.5kΩ, RX6 = 3.9kΩ, RX7 = 2kΩ, RX8 = 1kΩ, RX9 = 470Ω, RX10 = 240Ω, and RX11 = 120Ω. Some ratios are not entirely accurate, but to ensure low cost it is important to use only standard resistor values.
equation(16): using IVP = 11 obtain DF_LED ≈ 392
equation(17): DF_MO = 8
Table 2: FMS = '1', RB = 'Z', RA = '0'

## MEASURING THE PHASE SHIFT OF CURRENT TRANSFORMERS

The SA4301A derives the input current on the current sense networks directly from the current transformers. For this reason the actual phase shift added by the current transformer is usually less than the manufacturers specification. It is therefore advisable to measure the phase shift in application on a small sample of CTs. The best method to use is:

1. Design and implement the circuit using the procedure described. Assume ½ the manufactures specification for the phase shift of the CT when calculating the component values.
2. When assembling the PCB do not place the capacitors on the voltage sense networks.
3. Calibrate the meter at unity power factor using the procedure described in the “Calibrating the Meter” section. Ensure the error is as close to zero as possible.
4. Measure the error at power factor 0.5 lag and 0.5 lead for each phase individually. Ensure that the error is positive for 0.5 lag and negative for 0.5 lead. If this is not the case the phase shift of the CTs is too large or the cut-off frequency of the anti-alias filters on the current input networks is too high.
5. Obtain the average of the absolute values of the errors at 0.5 lag and 0.5 lead on all phases.
6. Using the result from step 5 calculate the overall phase shift of the current sensing network. This value is the phase shift of both the current transformer and the anti-alias filter combined and is equal to the required phase shift for the voltage sensing network:

$$\phi_{IV} = \phi_{II} + \phi_{CT} = 60^{o} - \arccos\left(0.5 \times \left(1 - \frac{\%Error}{100}\right)\right) \qquad (18)$$

7. Given the theoretical value of the current input network phase shift from equation (6) the value of $\phi_{CT}$ can be calculated.
8. Recalculate RX12 and RX13 and modify the PCB. Also add the voltage network compensation capacitors.
9. Recalibrate the meter and verify the performance at non-unity power factor.

## CALIBRATING THE METER

The RM4301ASEA is calibrated by means of a resistive ladder on the voltage sensing networks. The nine resistors can be chosen to represent any desired calibration range. The calibration accuracy can be extended by adding resistors to the ladder network. Soldering a jumper in parallel with a resistor closed will remove that resistor from the voltage divider network thereby providing a larger input current to the SA4301A and so increasing the output energy. The RM4301ASEA should be calibrated phase by phase with all three mains voltages present at all times. Each phase can be calibrated by first short circuiting resistor RX3. If the error is now positive a larger resistance is required so the jumper across RX3 is opened before proceeding to the next resistor in the network (RX4). If the error is negative then the process is simply continued with the next resistor. These steps are repeated for all nine resistors in the ladder network. The SA4301A is linear over the dynamic range required by the IEC62053-21 specification, so calibration is only required at one current value. Typically the basic current (Ib) is chosen as the calibration point. The repeatability of error measurements at Ib is typically better than 0.1% so the error of the meter can typically be measured accurately by a single integration of a very small number of pulses.

## PCB CONNECTIONS

The three CTs for phases 1 to 3 are connected to JA11A / JA11B, JB11A / JB11B and JC11A / JC11B respectively. The current transformers should be connected such that a positive current flows into JA11B, JB11B and JC11B when forward energy is applied to the meter. The three mains voltages should be connected to JA1, JB1 and JC1 respectively while the NEUTRAL line must be connected to J1. The opto-isolator output should be connectd to J2 while the stepper motor or impulse counter is connected to J3.

## JUMPER OPTIONS

The RM4301ASEA meter is equipped with several solderable selectors, which allow the meter to be set up according to the required specifications. Table 3 describes the functionality of the various jumpers. When working on the meter care should be taken to avoid electric shock due to the high voltages present.

| Name | Description |
|---|---|
| JA2 to JA10 | Used for calibration purposes of phase 1. Refer to the "Calibrating the Meter" section. |
| JB2 to JB10 | Used for calibration purposes of phase 2. Refer to the "Calibrating the Meter" section. |
| JC2 to JC10 | Used for calibration purposes of phase 3. Refer to the "Calibrating the Meter" section. |
| J4, J5 | Select the value of the RA pin. Only one connection should be closed at any time. To leave RA floating all connections must be opened. |
| J6, J7 | Select the value of the RB pin. Only one connection should be closed at any time. To leave RB floating all connections must be opened. |
| J8, J9 | Select the value of the MS pin. Only one connection should be closed at any time. To leave MS floating all connections must be opened. |
| J10 | Select the value of the FMS pin. Only one connection should be closed at any time. To leave FMS floating all connections must be opened. |

*Table 3: RM4301ASEA jumper options*

## EXTERNAL CONNECTIONS

The meter should be connected as shown in Table 4 and illustrated in Figure 6.

| Name | Function Description |
|---|---|
| 1 | LIVE IN PHASE 1: Live current input |
| 2 | VOLTAGE IN PHASE 1: Live voltage input if supplied separately. Can be connected directly to pin 1 by a movable link. |
| 3 | LIVE OUT PHASE 1: Live current output |
| 4 | LIVE IN PHASE 2: Live current input |
| 5 | VOLTAGE IN PHASE 2: Live voltage input if supplied separately. Can be connected directly to pin 4 by a movable link. |
| 6 | LIVE OUT PHASE 2: Live current output |
| 7 | LIVE IN PHASE 3: Live current input |
| 8 | VOLTAGE IN PHASE 3: Live voltage input if supplied separately. Can be connected directly to pin 7 by a movable link. |
| 9 | LIVE OUT PHASE 3: Live current output |
| 10 | NEUTRAL: Neutral voltage |
| + and - | Opto-isolated pulse output. This should be connected to the measurement or calibration equipment if no optical pickup is available. |

*Table 4: External connection description*

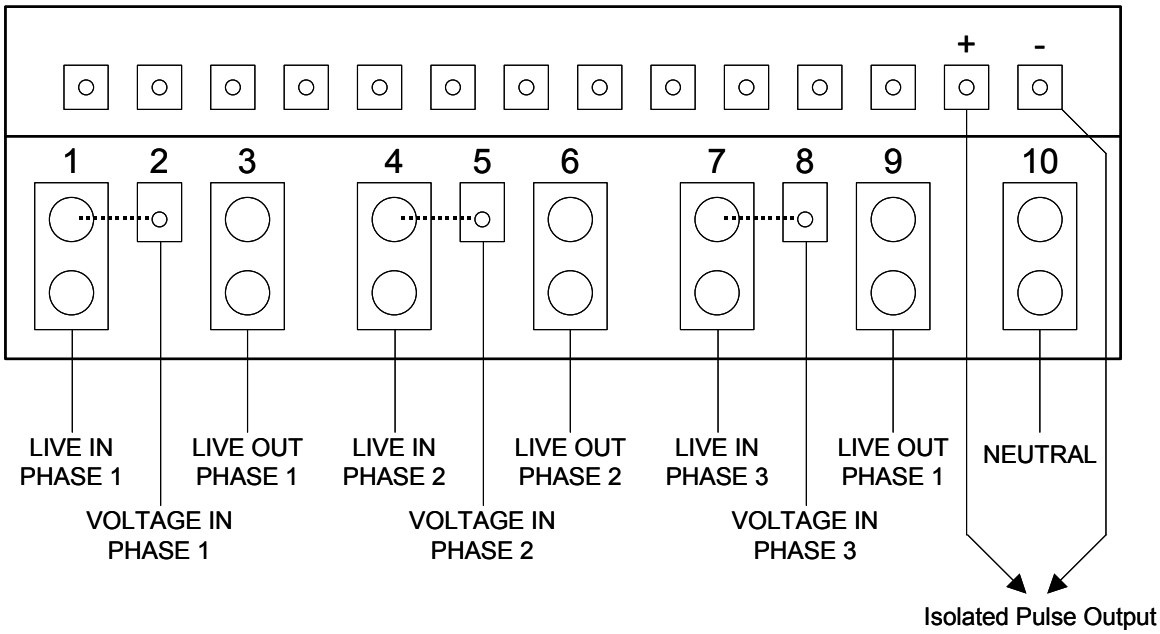


*Figure 6: External connection diagram for the RM4301ASEA meter*

## METER SCHEMATIC

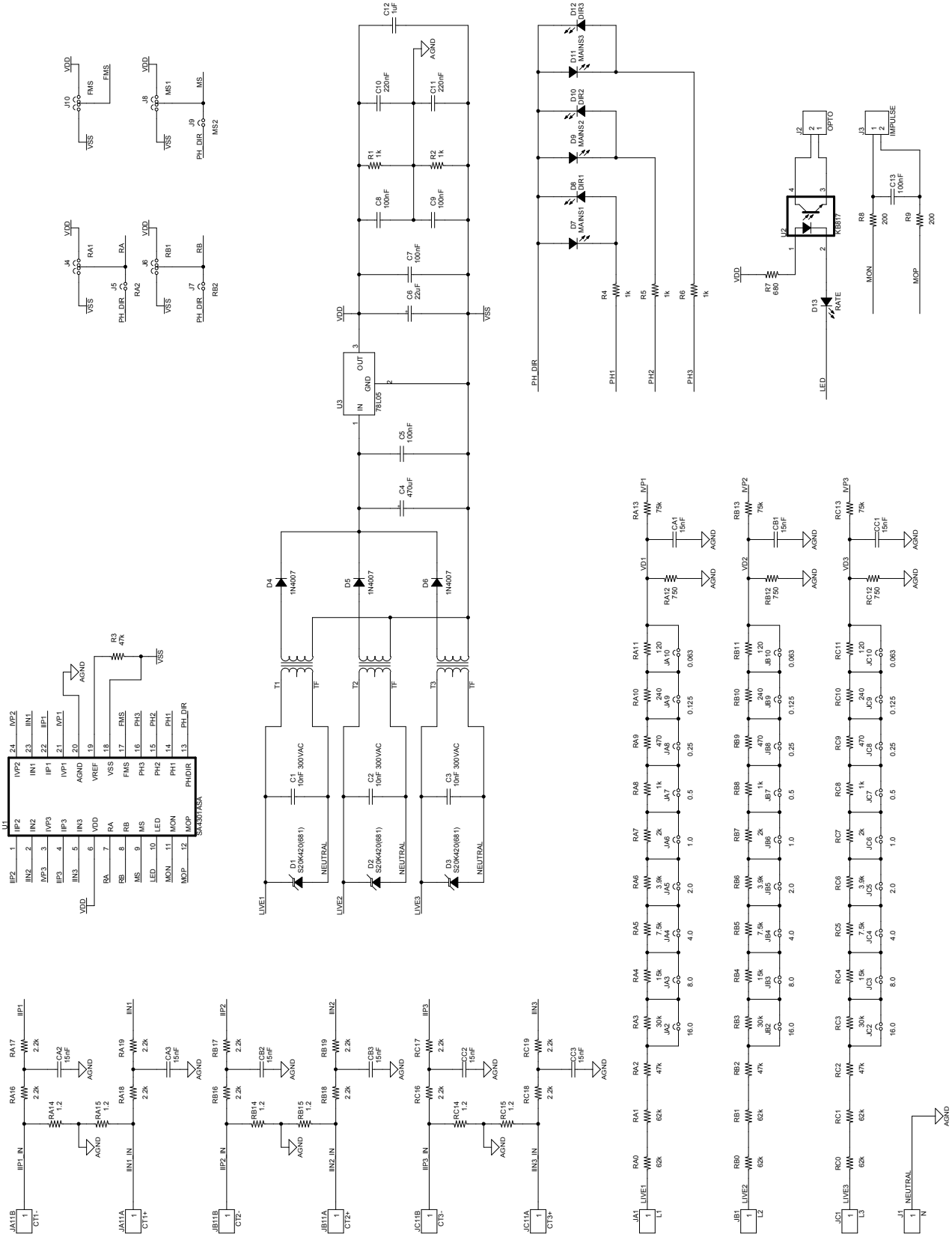

*Figure 7: Complete RM4301ASEA meter schematic*

## COMPONENT LIST

| Part | Detail | Description |
|---|---|---|
| C1, C2, C3 | 10nF, 300V, X2 | Metallized polyester film capacitor, leaded |
| C4 | 470µF, 25V | Capacitor, electrolytic radial, leaded |
| C6 | 22µF, 16V | Capacitor, electrolytic radial, leaded |
| C5, C7, C8, C9, C13 | 100nF | Capacitor, monolithic ceramic, SMD 0805 |
| C10, C11 | 220nF | Capacitor, monolithic ceramic, SMD 0805 |
| C12 | 1µF | Capacitor, monolithic ceramic, SMD 0805 |
| CA1, CA2, CA3, CB1, CB2, CB3 | 15nF | Capacitor, monolithic ceramic, SMD 0805 |
| CC1, CC2, CC3 | 15nF | Capacitor, monolithic ceramic, SMD 0805 |
| R1, R2, RA8, RB8, RC8 | 1kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| R3, RA2, RB2, RC2 | 47kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| R4, R5, R6 | 1kΩ | 1/8W, 5%, carbon resistor, SMD 0805 |
| R7 | 680Ω | 1/8W, 5%, carbon resistor, SMD 0805 |
| R8, R9 | 200Ω | 1/8W, 5%, carbon resistor, SMD 0805 |
| RA0, RA1, RB0, RB1, RC0, RC1 | 62kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA3, RB3, RC3 | 30kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA4, RB4, RC4 | 15kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA5, RB5, RC5 | 7.5kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA6, RB6, RC6 | 3.9kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA7, RB7, RC7 | 2kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA9, RB9, RC9 | 470Ω | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA10, RB10, RC10 | 240Ω | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA11, RB11, RC11 | 120Ω | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA12, RB12, RC12 | 750Ω | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA13, RB13, RC13 | 75kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RA14, RA15, RB14, RB15, RC14, RC15 | 1.2Ω | 1/4W, 1%, metal film resistor, axial, leaded |
| RA16, RA17, RA18, RA19, RB16, RB17, | 2.2kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| RB18, RB19, RC16, RC17, RC18, RC19 | 2.2kΩ | 1/8W, 1%, metal film resistor, SMD 0805 |
| D1, D2, D3 | S20K420(681) | Metal oxide varistor |
| D4, D5, D6 | 1N4007 | Rectifier diode, leaded |
| D7, D9, D11 | LED | 3mm, Green |
| D8, D10, D12 | LED | 3mm, Yellow |
| D13 | LED | 3mm, Red |
| U1 | SA4301A | Energy meter device, 24-pin SOIC, 0.8mm |
| U2 | KB817 | Opto-isolator, 4-pin PDIP, 2.54mm |
| U3 | 78L05 | 5V, Regulator TO-22 |
| T1, T2, T3 | Transformer | 0-11-220V primary / 11V secondary |

*Table 5: Component list for the RM4301ASEA meter*

## TYPICAL PERFORMANCE CURVES

The following performance curves show typical results obtained with several RM4301ASEA meters.

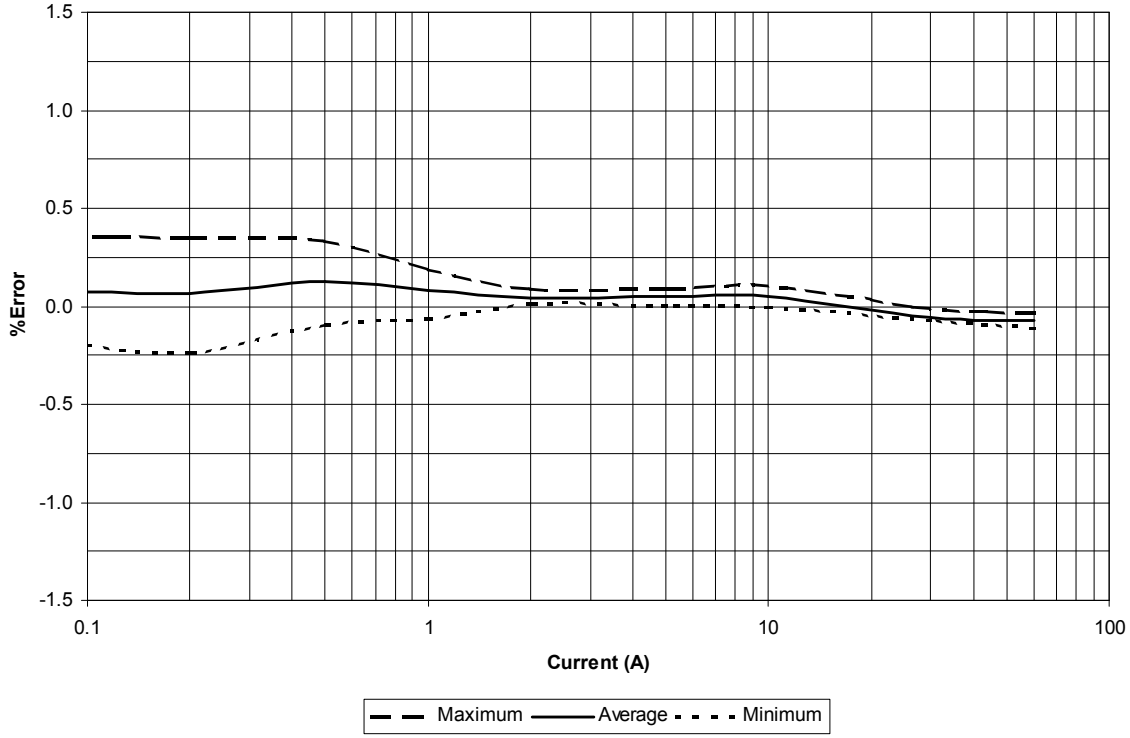


*Figure 8: Typical performance of the RM4301ASEA at balanced load and unity power factor*

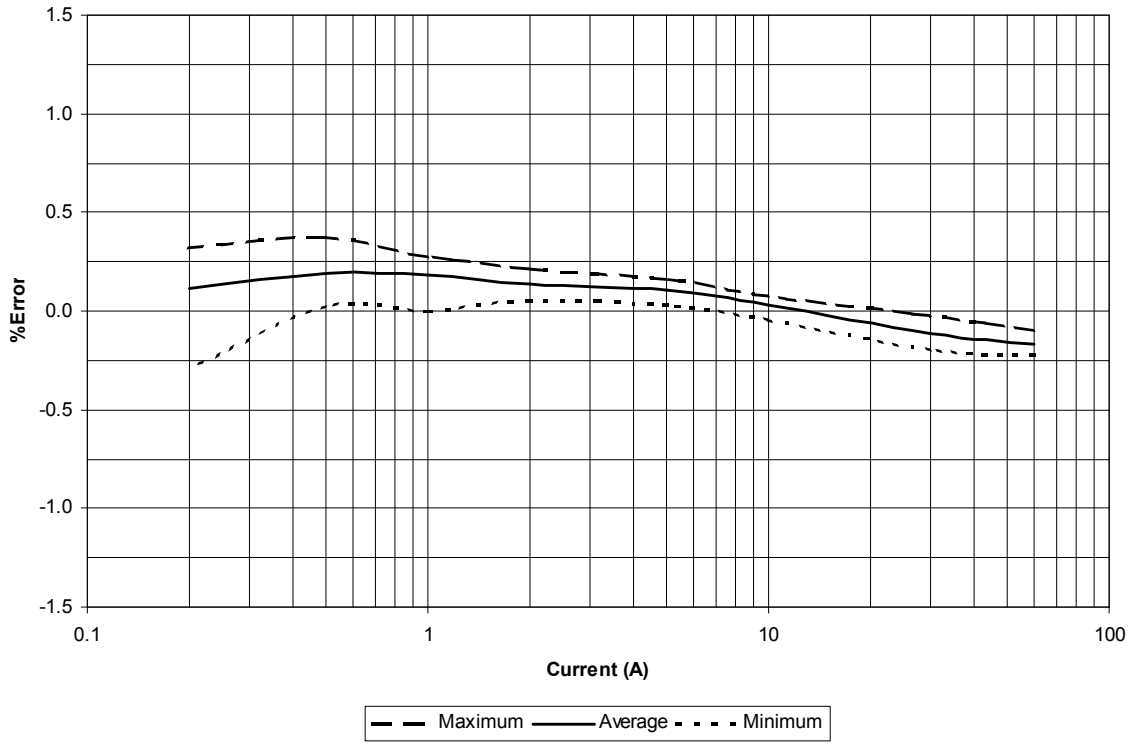


*Figure 9: Typical performance of the RM4301ASEA at balanced load and 0.5 lag power factor*

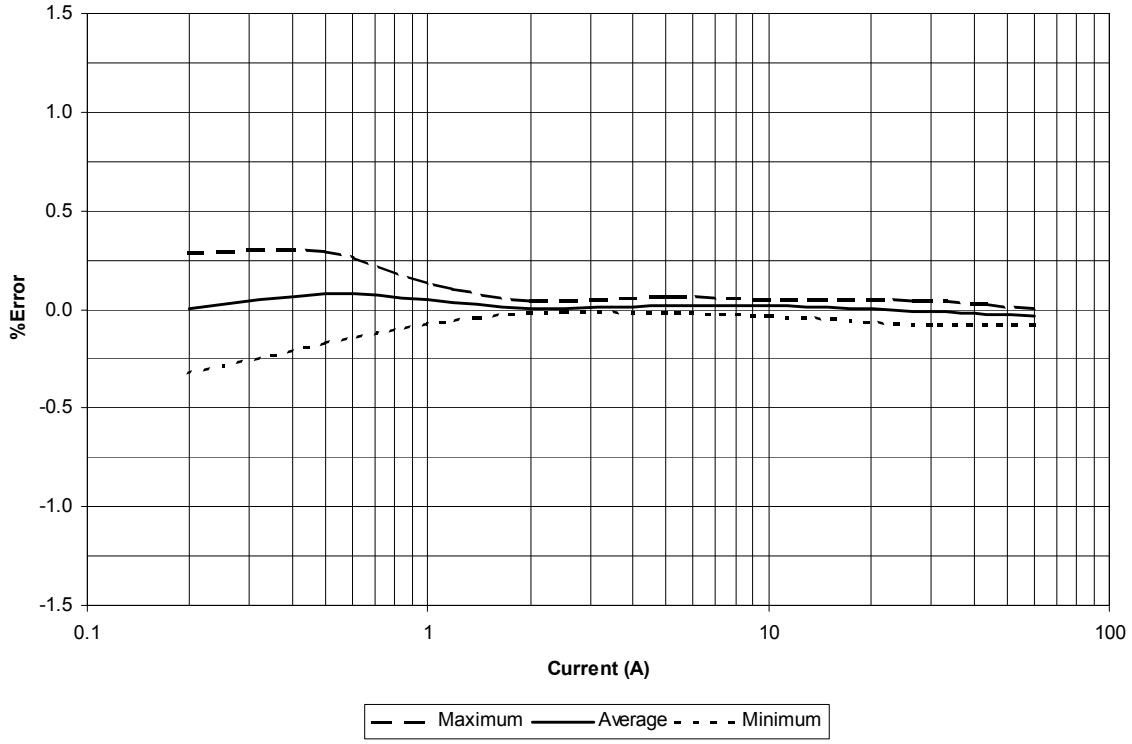


*Figure 10: Typical performance of the RM4301ASEA at balanced load and 0.8 lead power factor*

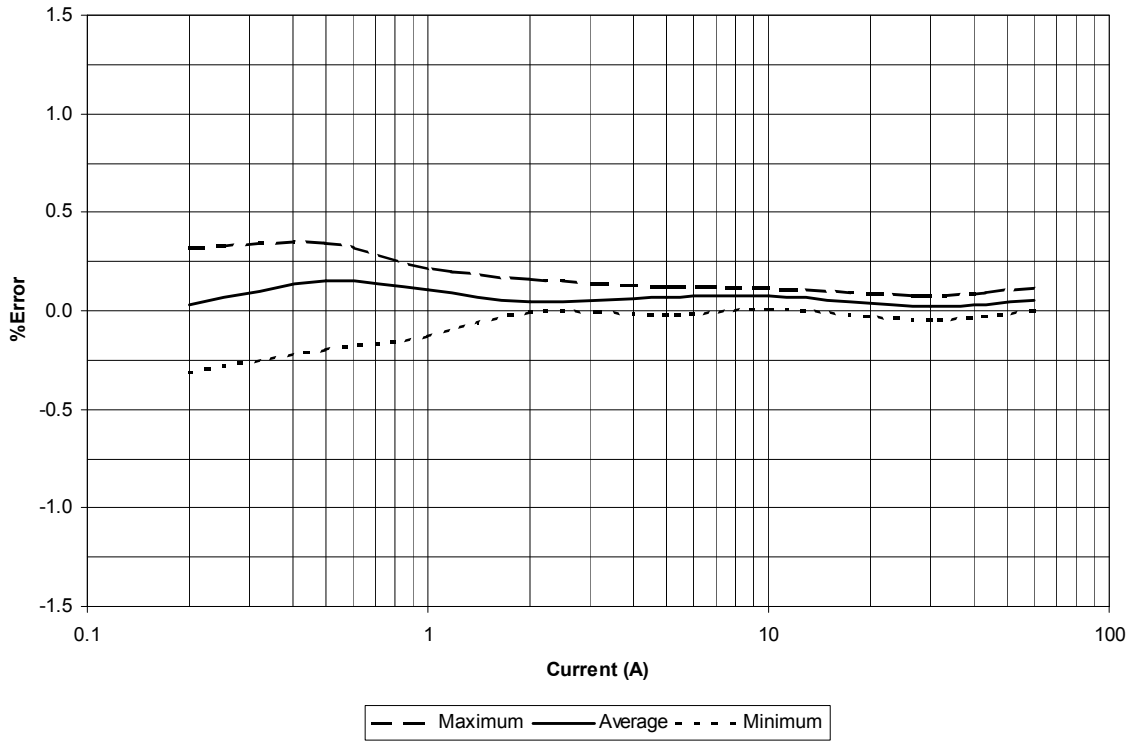


*Figure 11: Typical performance of the RM4301ASEA at single phase load and unity power factor*

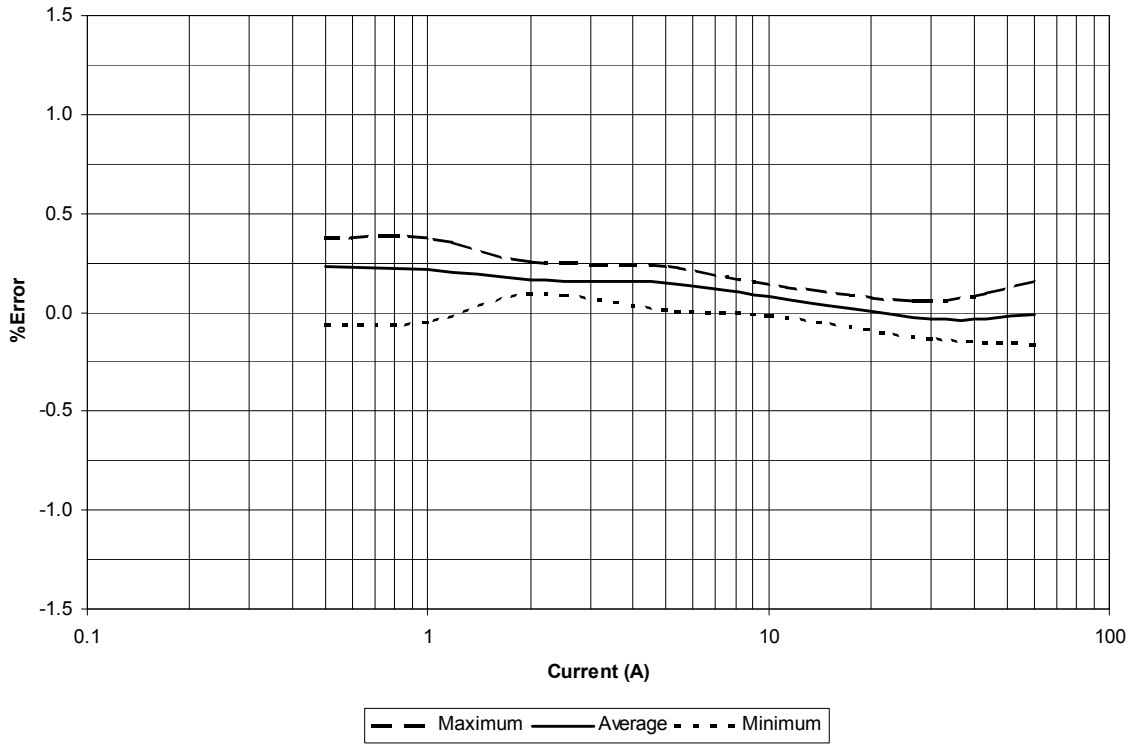


*Figure 12: Typical performance of the RM4301ASEA at single phase load and 0.5 lag power factor*

## PCB LAYOUT

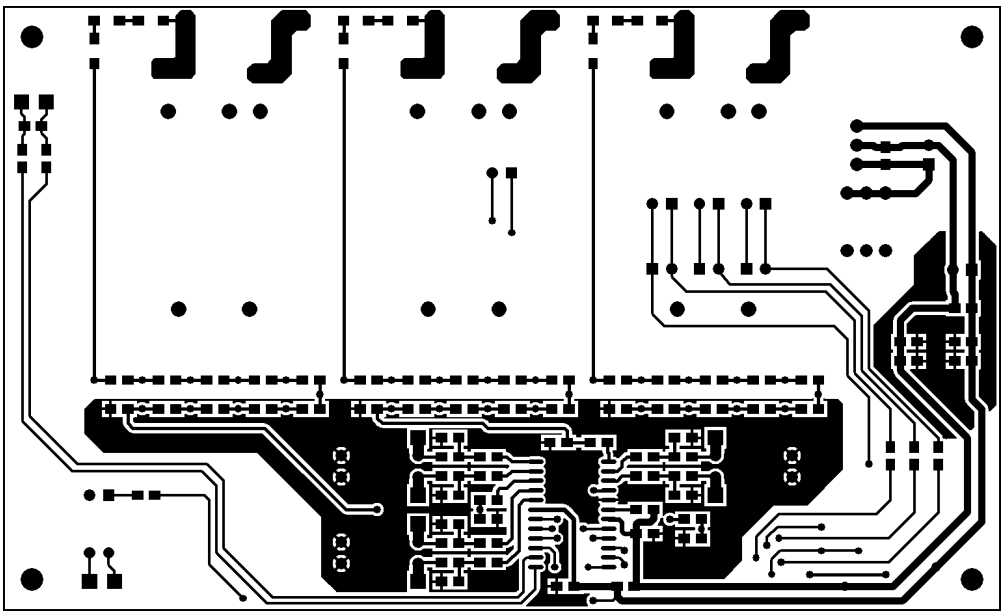

*Figure 13: PCB Top Layer (Scale 1:1)*

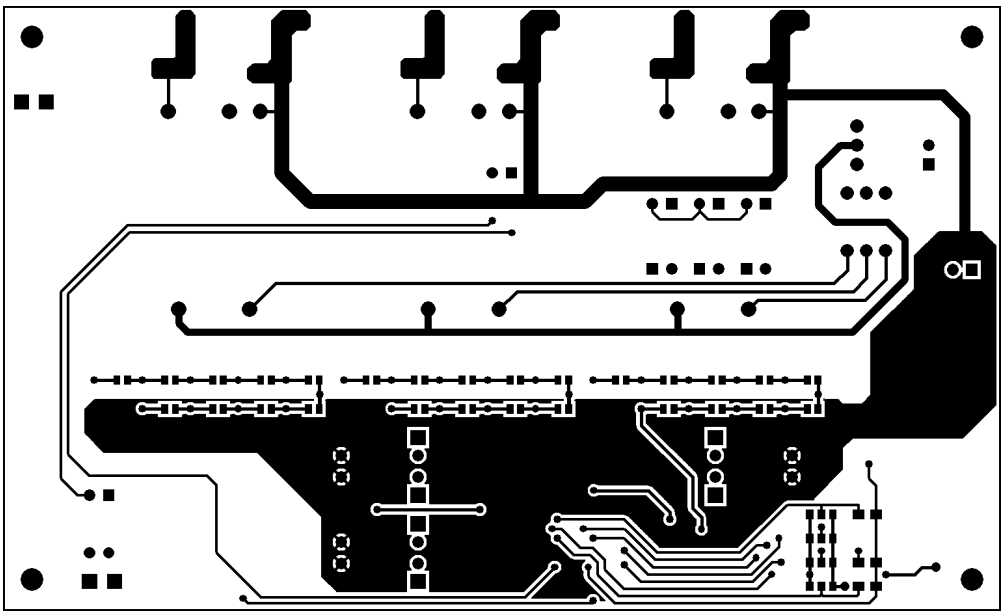

*Figure 14: PCB Bottom Layer (Scale 1:1)*

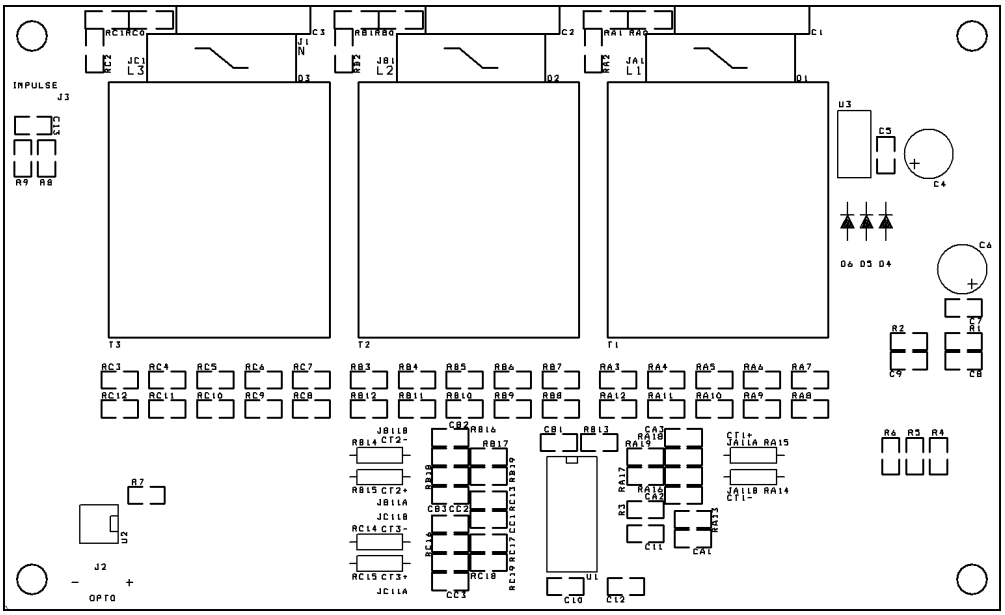

*Figure 15: PCB Silkscreen Top Layer (Scale 1:1)*

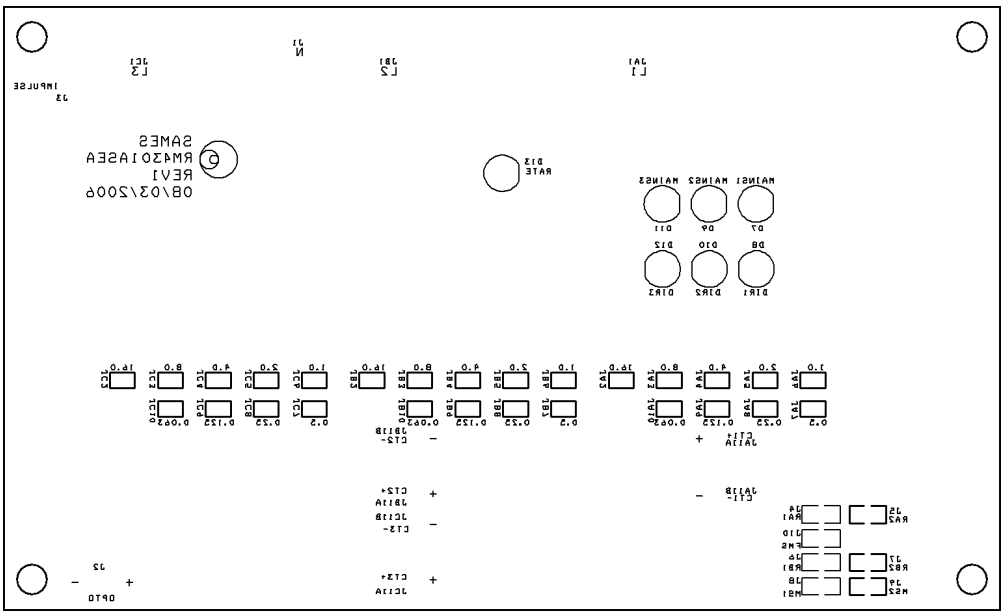

*Figure 16: PCB Silkscreen Bottom Layer (Scale 1:1)*

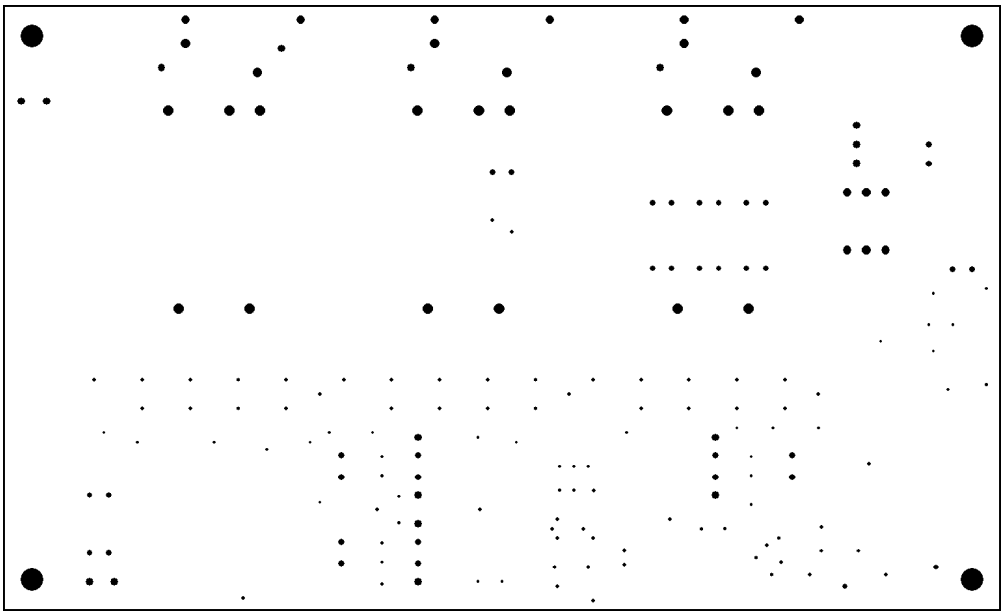

*Figure 17: PCB Drill Drawing Top/Bottom Layer (Scale 1:1)*

## NOTES

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