Three Phase Bidirectional Energy Metering IC with Instantaneous Frequency Output

SA4305A

FEATURES

- Meets the IEC62053, CBIP-88 and IS137799-1999 specification requirements for Class 1 AC static watt-hour meters for active energy
- Pulse output supplies instantaneous active power information
- Bidirectional three phase power and energy measurement
- Precision on-chip oscillator (70ppm/°C drift)
- Precision on-chip voltage reference (10ppm/°C drift)
- Integrated anti-creep function per channel
- Low power consumption (<40mW typical)
- Measures AC inputs only
- Functionally compatible with SA2005F

DESCRIPTION

The SA4305A is an accurate three phase power/energy metering integrated circuit providing a single chip solution for three phase energy metering. Very few external components are required and the SA4305A does not require an external crystal or voltage reference. A precision oscillator and a precision voltage reference to supply the circuitry with a stable frequency and stable reference currents are integrated on the chip.

The SA4305A metering integrated circuit generates a pulse output, the frequency of which is proportional to the instantaneous active power consumption. The pulse output is intended to interface with a microcontroller or similar pulse counting circuitry.

The SA4305A includes an anti-creep feature preventing any creep effects that affect meter accuracy under no-load or missing phase conditions.

The SA4305A integrated circuit is available in a 20 pin small outline (SOIC20) RoHS compliant package.

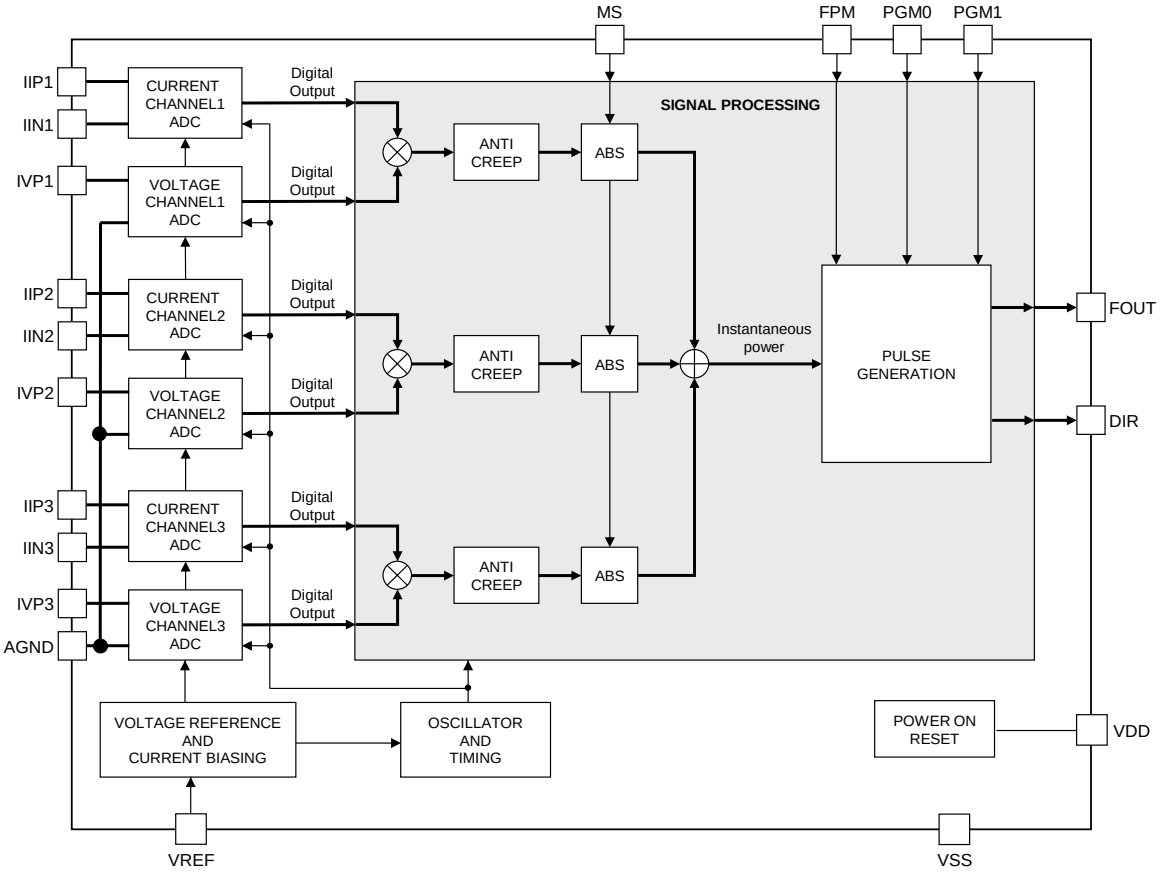


Figure 1: Block diagram

ELECTRICAL CHARACTERISTICS

(V_{DD} - V_{SS} = 5V ± 10%, over the temperature range -40°C to +85°C, unless otherwise specified. Refer to Figure 2 “Test circuit for electrical characteristics”.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
General						
Supply Voltage: Positive	V_{DD}	2.25	2.5	2.75	V	With respect to AGND
Supply Voltage: Negative	V_{SS}	-2.75	-2.5	-2.25	V	With respect to AGND
Supply Current: Positive	I_{DD}		7.5	10.5	mA	
Supply Current: Negative	I_{SS}		-7.5	-10.5	mA	
Analog Inputs						
Current Sensor Inputs (Differential)						
Input Current Range	IR_{IIP1}, IR_{IIP2}, IR_{IIP3}, IR_{IIN1}, IR_{IIN2}, IR_{IIN3}	-25		25	µA	Peak value
Offset Voltage	VO_{IIP1}, VO_{IIP2}, VO_{IIP3}, VO_{IIN1}, VO_{IIN2}, VO_{IIN3}	-4		4	mV	With R = 4.7kΩ connected to AGND
Voltage Sensor Inputs (Asymmetrical)						
Input Current Range	IR_{IVP1}, IR_{IVP2}, IR_{IVP3}	-25		25	µA	Peak value
Offset Voltage	VO_{IVP1}, VO_{IVP2}, VO_{IVP3}	-4		4	mV	With R = 4.7kΩ connected to AGND
Digital Inputs						
PGM0, PGM1, FPM, MS Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	 V_{DD}-1		 V_{SS}+1	 V V	
FPM, MS Pull-down current	I_{PD}	40		200	µA	
Digital Outputs						
FOUT Output Frequency	F_{MAX}	1.04	1.16	1.27	kHz	At rated input conditions: 14µA_{RMS} on voltage channels, 16µA_{RMS} on current channels, MODE 3
FOUT, DIR Output High Voltage Output Low Voltage	 V_{OH} V_{OL}	 V_{DD}-1		 V_{SS}+1	 V V	 I_{SOURCE} = 5mA I_{SINK} = 5mA

During manufacturing, testing and shipment we take great care to protect our products against potential external environmental damage such as Electrostatic Discharge (ESD). Although our products have ESD protection circuitry, permanent damage may occur on products subjected to high-energy electrostatic discharges accumulated on the human body and/or test equipment that can discharge without detection. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality during product handling.

ATTENTION: Electrostatic sensitive device. Requires special handling.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} - V_{SS} = 5V ± 10%, over the temperature range -40°C to +85°C, unless otherwise specified. Refer to Figure 2 “Test circuit for electrical characteristics”.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
On-chip Voltage Reference						
Reference Voltage	V_R	1.15	1.20	1.25	V	
Reference Current	$-I_R$	24.4	25.5	26.6	µA	With R = 47kΩ connected to V_{SS}
Temperature Coefficient	TC_R		10	70	ppm/ºC	
On-chip Oscillator						
Oscillator Frequency	f_{OSC}	3.15	3.57	4.00	MHz	
Temperature Coefficient	TC_{OSC}		70	200	ppm/ºC	

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD} - V_{SS}		6	V
Current on any Pin	I_{PIN}	-150	150	mA
Storage Temperature	T_{STG}	-60	+125	ºC
Specified Operating Temperature Range	T_O	-40	+85	ºC
Limit Range of Operating Temperature	T_{limit}	-40	+85	ºC

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operational sections of this specification, is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

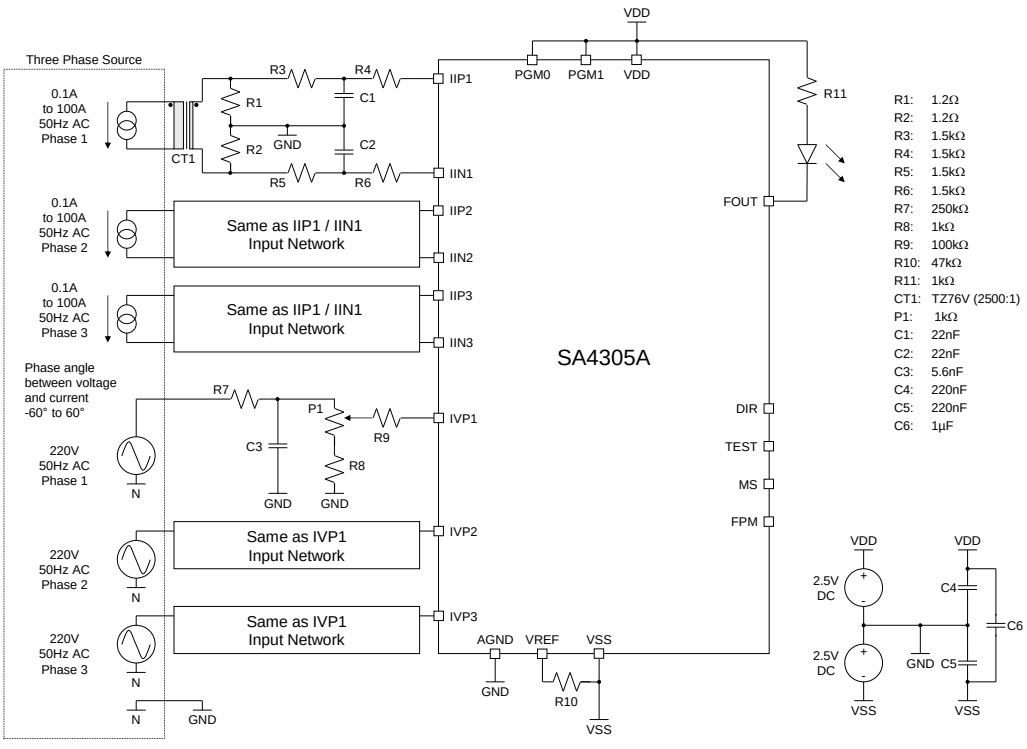


Figure 2: Test circuit for electrical characteristics

PIN DESCRIPTION

Designation	Pin No.	Description
AGND	16	Analog Ground. This is the reference pin for the current and voltage signal sensing networks. The supply voltage to this pin should be mid-way between V_{DD} and V_{SS}.
VDD	6	Positive Supply Voltage. The voltage to this pin should be +2.5V ± 10% with respect to AGND.
VSS	14	Negative Supply Voltage. The voltage to this pin should be -2.5V ± 10% with respect to AGND.
IVP1, IVP2, IVP3	17, 20, 3	Analog Inputs for Voltages. The maximum current into the voltage sense inputs IVP should not exceed 16μA_{RMS}. At nominal voltage an input current of 14μA_{RMS} is recommended. The voltage sense inputs saturate at an input current of ±25µA peak.
IIP1, IIN1, IIP2, IIN2, IIP3, IIN3	18, 19, 1, 2, 4, 5	Analog Inputs for Currents. The maximum current into the current sense inputs IIP/IIN should be set at 16μA_{RMS}. The current sense inputs saturate at an input current of ±25µA peak.
VREF	15	This pin provides the connection for the reference current setting resistor. A 47kΩ resistor connected to V_{SS} sets the optimum operating conditions.
FOUT	8	Pulse output. Refer to the Pulse Output section for information on the pulse output
DIR	9	Direction Indicator output. This output indicates the direction of energy flow.
PGM0, PGM1	12, 13	Pulse Output Format Selection inputs. These input pins define the pulse output format. Refer to the Pulse Output Format section for more information.
MS	11	Adder Mode Select input. Controls the mode of the pulse adder.
FPM	10	Fast Pulse Mode Select input. Controls the high frequency pulse output mode.
TEST	7	Manufacturers test pin. This pin should remain unconnected.

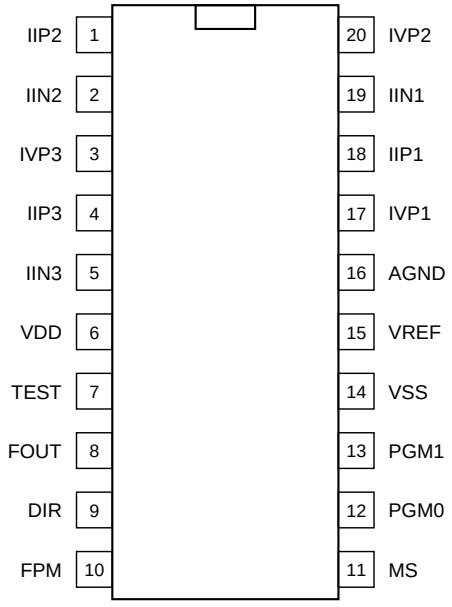


Figure 3: Pin connections

ORDERING INFORMATION

Part Number	Package
SA4305ASAR	SOIC20 (RoHS compliant)

TERMINOLOGY

Anti-Creep Threshold

The anti-creep threshold is defined as the minimum energy threshold below which no energy is registered and therefore no pulses are generated on the pulse output.

Positive Energy

Positive energy is defined when the phase difference between the input signals IIP and IVP is less than 90 degrees (-90..90 degrees).

Negative Energy

Negative energy is defined when the phase difference between the input signals IIP and IVP is greater than 90 degrees (90..270 degrees).

Percentage Error*

Percentage error is given by the following formula:

$$\%Error = \frac{Energy\ registered - True\ Energy}{True\ Energy} \times 100$$

NOTE: Since the true value cannot be determined, it is approximated by a value with a stated uncertainty that can be traced to standards agreed upon between manufacturer and user or to national standards.

Rated Operating Conditions*

Set of specified measuring ranges for performance characteristics and specified operating ranges for influence quantities, within which the variations or operating errors of a meter are specified and determined.

Specified Measuring Range*

Set of values of a measured quantity for which the error of a meter is intended to lie within specified limits.

Specified Operating Range*

A range of values of a single influence quantity, which forms a part of the rated operating conditions.

Limit Range of Operation*

Extreme conditions which an operating meter can withstand without damage and without degradation of its metrological characteristics when it is subsequently operated under its rated operating conditions.

Maximum Rated Mains Current (I_{MAX})

Maximum rated mains current is the specified maximum current flowing through the energy meter at rated operating conditions.

Constant*

Value expressing the relation between the active energy registered by the meter and the corresponding value of the test output. If this value is a number of pulses, the constant should be either pulses per kilowatt-hour (imp/kWh) or watt-hours per pulse (Wh/imp).

Nominal Mains Voltage (V_{NOM})

Nominal mains voltage (V_{NOM}) is the voltage specified for the energy meter at rated operating conditions.

Maximum Channel Energy (E_{MAX})

The maximum channel energy is defined as the energy registered on one channel of the SA4305A when 14μA_{RMS} and 16μA_{RMS} input current with zero phase shift are applied to the voltage and current inputs respectively. Both the voltage and current inputs saturate at an input current magnitude of 25μA, or at 17.68μA_{RMS} when using sine waves. The maximum input current on each channel is therefore defined to be 16μA_{RMS}, which leaves about 10% headroom to the saturation point. An additional headroom of 15% is reserved on the voltage channel to account for mains voltage fluctuations.

Maximum Output Frequency (F_{MAX})

The maximum output frequency (F_{MAX}) is the output frequency when 14μA_{RMS} and 16μA_{RMS} input current with zero phase shift are applied to the voltage and current inputs of all three channels respectively. Both the voltage and current inputs saturate at an input current magnitude of 25μA, or at 17.68μA_{RMS} when using sine waves. The maximum input current on any channel is therefore defined to be 16μA_{RMS}, which leaves about 10% headroom to the saturation point. An additional headroom of 15% is reserved on the voltage channels to account for mains voltage fluctuations. The nominal output frequency of 1160Hz is achieved under such conditions.

* IEC 62052-11, 2003. Electricity Metering Equipment (AC) – General Requirements, Test and Test Conditions – Part 11: Metering Equipment

PERFORMANCE GRAPHS

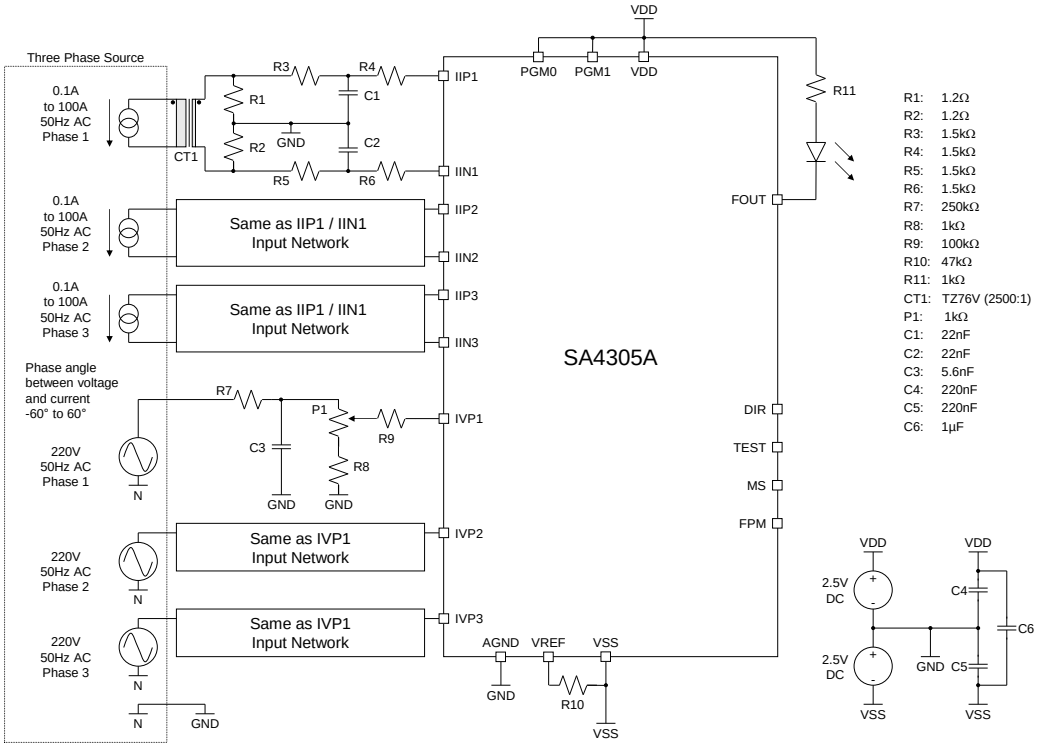
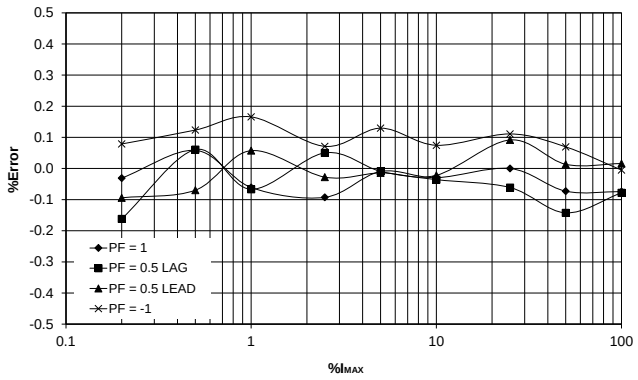
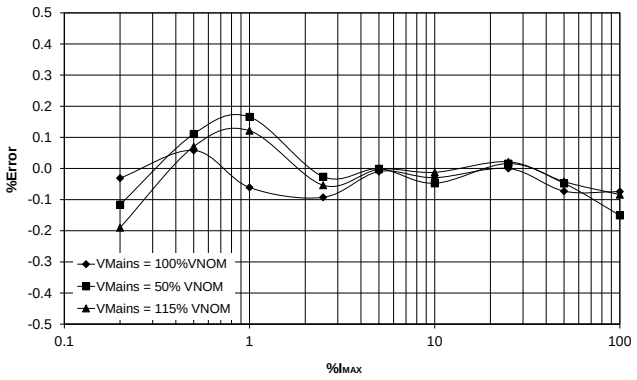


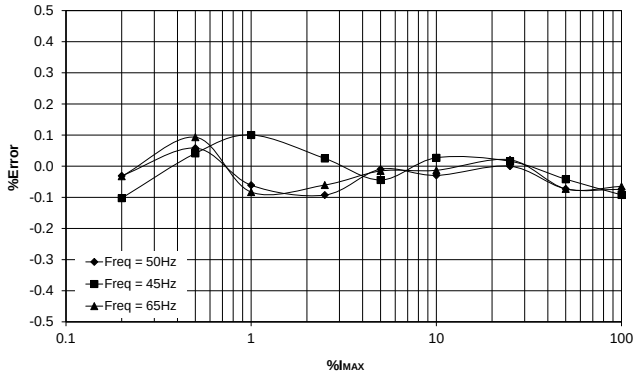
Figure 4: Test circuit for performance graphs



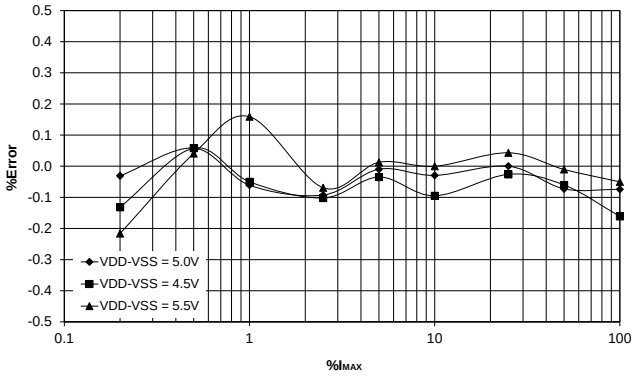
Graph 1: Freq = 50Hz, VMains = V_{NOM}, Temp = 25°C, V_{DD}-V_{SS} = 5.0V



Graph 2: PF = 1, Freq = 50Hz, Temp = 25°C, V_{DD}-V_{SS} = 5.0V



Graph 3: PF = 1, VMains = V_{NOM}, Temp = 25°C, V_{DD}-V_{SS} = 5.0V



Graph 4: PF = 1, Freq = 50Hz, VMains = V_{NOM}, Temp = 25°C

FUNCTIONAL DESCRIPTION

Theory of Operation

The SA4305A includes all the required functions for three phase power and energy measurement. Three pairs of identical AD converters sample the three phase voltage and current input signals. The three pairs of digital signals, accurately representing the voltage and current inputs, are multiplied using digital multiplication. The output of each multiplier represents the instantaneous power on each channel. The three channels are added together and the pulse generation circuit creates a pulse output where the instantaneous frequency is proportional to the instantaneous power measured. The addition of the three channels can be programmed to arithmetic or absolute mode. The arithmetic mode will take the direction of energy flow into account while the absolute mode will ignore it.

For given voltage and current signals the instantaneous power is calculated by:

$$p(t) = v(t) \times i(t)$$
$$p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \psi)$$

Let $\phi = \theta - \psi$, and $V_{RMS} = \frac{V_M}{\sqrt{2}}$ and $I_{RMS} = \frac{I_M}{\sqrt{2}}$ then

$$p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \theta - \phi)$$
$$p(t) = V_{RMS} I_{RMS} (\cos\phi + \cos(2(\omega t + \theta) - \phi))$$

where
p(t) is the instantaneous power,
v(t) is the instantaneous voltage signal,
i(t) is the instantaneous current signal,
V_M is the amplitude of the voltage signal,
I_M is the amplitude of the current signal,
θ is the phase angle of the voltage signal and
ψ is the phase angle of the current signal.

The instantaneous power output is integrated over time to obtain the energy by simply counting the output pulses. This removes the double mains frequency component cos(2(ωt+θ)-ϕ) and the average output pulse rate is therefore equivalent to

$$P = \frac{1}{T} \int_0^T p(t) dt$$
$$P = V_{RMS} I_{RMS} \cos\phi$$

where
P is the average power and
$cos\phi$ is the power factor.

Linearity

The SA4305A is a CMOS integrated circuit, which performs power/energy calculations across a dynamic range of 500:1 to an accuracy that exceeds the IEC62053 specification.

Analog Inputs

The input circuitry of the current and voltage sensor inputs is illustrated in Figure 5. These inputs are protected against electrostatic discharge through clamping diodes. The feedback loops from the outputs of the amplifiers A_I and A_V generate virtual short circuits between IIP and IIN as well as IVP and AGND. The current sense inputs (IIP and IIN) are identical and balanced. The AD converters convert the signals on the voltage and current sense inputs to a digital format for further processing. All internal offsets are eliminated through the use of various cancellation techniques.

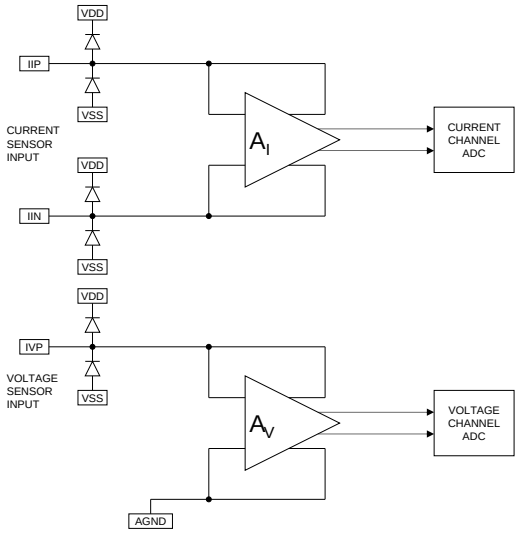


Figure 5: Analog input configuration

Digital Outputs

The calculations required for power and energy are performed and the result is converted to pulses on the FOUT pulse output. The instantaneous output frequency on the pulse output is proportional to the instantaneous active power consumption measured. The pulse output is intended for interfacing the SA4305A to a microcontroller or similar pulse processing circuit.

Anti-Creep Threshold

An integrated anti-creep function prevents any output pulses from a channel appearing on the pulse output if the energy measured on that channel is less than 0.02% of E_{MAX}, where E_{MAX} is the energy registered when the input currents for voltage and current are 14μA_{RMS} and 16μA_{RMS} with zero phase shift respectively. The individual per channel creep

feature improves the device performance in missing phase scenarios. It also allows the device to be used in three phase three wire meters where one channel of the device is unused.

Reverse Energy Flow Indication

The SA4305A assesses the phase difference between the voltage and current channel signals to determine the direction of energy flow. If the overall energy flow is negative the reverse energy indicator is activated. This facility is designed to detect the wrongful connection or possible tampering of the meter. If the adder is programmed to absolute mode the energy flow direction information is lost. The operation of the direction output is fully described in the Output Signals section.

Starting Current

The SA4305A generates pulses on the pulse outputs for an input power greater than 0.02% of E_{MAX}. This is to comply with the IEC requirement where the meter is required to generate pulses for currents greater than 0.4%Ib.

Power-On Reset

The SA4305A has a power-on reset circuitry that activates whenever the voltage between VDD and VSS is less than 3.6V ± 8%.

Power Consumption

The power consumption of the SA4305A integrated circuit is less than 50mW.

Compatibility with SA2005F

The SA4305A can be used as a functionally compatible replacement for the SA2005F by simply leaving the pins FPM and MS unconnected. It should however be noted that the value of the reference resistor on the VREF pin has to be changed from 24kΩ to 47kΩ.

INPUT SIGNALS

Voltage Reference (VREF)

A bias resistor of 47kΩ sets optimum bias and reference conditions on chip. Calibration of the SA4305A should be done on the voltage inputs and not on the VREF input.

Current Sense Inputs (IIP1/IIN1, IIP2/IIN2, IIP3/IIN3)

Figure 6 shows the typical connections for the current sensor input for one channel. The circuit has to be repeated for the other two channels. At maximum rated mains current (I_{MAX}) the resistor values should be selected for input currents of $16\mu A_{RMS}$. The current sense inputs saturate at an input current of $\pm 17.6\mu A_{RMS}$ ($\pm 25\mu A_{PEAK}$), so this allows about 10% headroom until saturation occurs.

The resistors RA and RB form the current transformers termination resistor. The reference level is connected in the centre of the termination resistor to achieve purely differential input currents. The voltage drop across the termination resistors at maximum rated mains current (I_{MAX}) should be in the order of $100mV_{RMS}$. The termination resistance should also be significantly smaller than the DC resistance of the current transformers secondary winding.

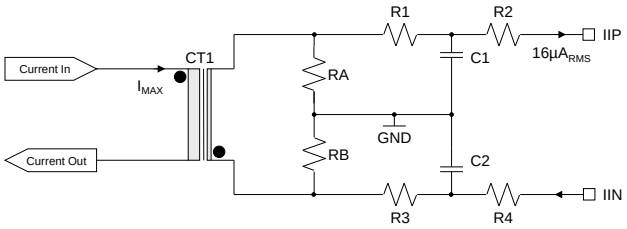


Figure 6: Current sense input configuration

The resistors R1 to R4 define the current flowing into the device. For best performance the SA4305A requires anti-alias filters on the current sense inputs. These filters are realized by means of the capacitors C1 and C2. The typical cut-off frequency of these filters should be between 10kHz and 20kHz. The optimum input network is achieved by setting the input resistors equal, i.e. setting R1 = R2 = R3 = R4 = R_C. This sets the equivalent resistance associated with each capacitor to $R_C/2$.

Voltage Sense Inputs (IVP1, IVP2, IVP3)

Figure 7 shows the voltage sense input configuration for one channel. The circuit is identical for the other two channels. The voltage sense input saturates at an input current of $\pm 17.6\mu A_{RMS}$ ($\pm 25\mu A_{PEAK}$). The current into the voltage sense input should be set at $14\mu A_{RMS}$ at nominal mains voltage (V_{NOM}) to allow for a mains voltage variation of up to +25% without saturating the voltage sense input.

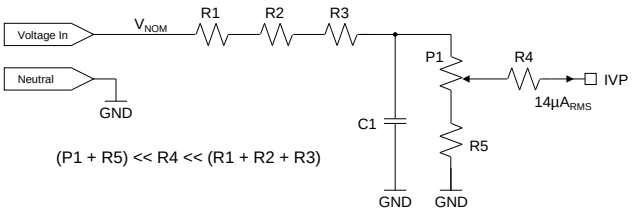


Figure 7: Voltage sense input configuration

For best performance the SA4305A also requires an anti-alias filter on the voltage sense inputs. Referring to Figure 7, the capacitor C1 is used to both implement the anti-alias filter as well as compensating for any phase shift caused by the current transformer. The resistor R4 defines the input current into the device. The optimum input network is achieved by setting R4 in the order of 100kΩ. If R4 is made too large the capacitor C1 will be very small and the accuracy of the phase

compensation could be affected by stray capacitances. The potentiometer P1 is used for calibration purposes.

Pulse Output Format Selection (PGM0, PGM1, FPM)

The pulse output programming inputs PGM0, PGM1 and FPM define the representation of energy measured by the device on FOUT. Table 1 below shows the difference between the various modes. Mode 4 basically bypasses the adder and the individual pulses of each channel of the device are output directly. The pulse width allows the allocation of pulses to specific channels. Refer to Table 1 for details on the pulse output format in each mode.

Adder Mode Selection (MS)

The energy addition of the three channels may be set to arithmetic or absolute mode using the MS input. If MS is tied to V_{SS} the adder operates in arithmetic mode. In this mode the direction of energy flow on each channel is taken into account during addition. Negative energy is thus subtracted from positive energy in the addition process. If MS is tied to V_{DD} the adder operates in absolute mode. The direction of energy flow on each channel is ignored and assumed to be positive. The reversal of a channel will therefore not affect the pulse output rate. This can be used as an anti-tamper feature. The MS input is ignored in pulse output mode 4 where the pulses on each channel are output individually.

OUTPUT SIGNALS

Pulse Output (FOUT)

The average nominal output frequency of the pulse output in mode 3 is given by

$$f_{FOUT-MODE3} = 1160 \times \left| \frac{IV_1 \times II_1 \times \cos\phi_1 + IV_2 \times II_2 \times \cos\phi_2 + IV_3 \times II_3 \times \cos\phi_3}{3 \times 14 \times 16} \right| \quad \ldots(1)$$

where

IV_X and II_X are the analog input currents in μA_{RMS} on the voltage and current sense inputs on channel X and

ϕ_X is the phase angle between the current and voltage signals on channel X.

The pulse output rate in modes 0, 1 and 2 is 18 times lower than in mode 3 and 4. The integrated anti-creep threshold ensures that no output pulses are generated from a channel if the energy measured on that channel is below 0.02% of E_{MAX}, where E_{MAX} is the energy registered on the channel when the voltage and current sense input currents are $14\mu A_{RMS}$ and $16\mu A_{RMS}$ respectively. The power-up state of the pulse output is dependent on the pulse output mode that has been selected.

Figure 8 shows the output waveform of FOUT for the pulse output modes 0 to 3. Modes 0, 1 and 2 allow direct sensing of the total energy flow direction from the pulse output. Note that the pulse output timing and rate differ in mode 3. This fact has been omitted in Figure 8 for the sake of clarity. Setting FPM, PGM0 and PGM1 to V_{DD} will set the pulse output mode to mode 4. In this mode the internal pulse adder is bypassed. Each channel's pulses appear independently on FOUT. The pulse width allows the output pulses to be allocated to a specific channel. The pulses from channel 2 are 1.5x the width of the channel 1 pulses while those of channel 3 are 2x the width of the channel 1 pulses. Pulse output mode 4 is illustrated in Figure 9.

Table 1: Pulse output characteristics for various modes

Mode	FPM	PGM1	PGM0	Frequency at rated conditions	Forward energy pulse polarity	Reverse energy pulse polarity	Pulse on direction change	Forward energy pulse width	Reverse energy pulse width
0	X	0	0	64.4Hz	Positive	Positive	Yes	1.15ms	3.44ms
1	X	0	1	64.4Hz	Positive	Negative	Yes	1.15ms	1.15ms
2	X	1	0	64.4Hz	Positive	Negative	No	1.15ms	1.15ms
3	0	1	1	1160Hz	Negative	Negative	Yes	71.7µs	71.7µs
4	1	1	1	386Hz per channel	Negative	Negative	Yes	71.7µs Ch1 108µs Ch2 143us Ch3	71.7µs Ch1 108µs Ch2 143us Ch3

Notes:
1. Pin values for FPM, PGM0 and PGM1, 0 means pin is connected to V_{SS}, 1 means pin is connected to V_{DD}, X means the pin state is irrelevant
2. Pulse rate of modes 3 and 4 is 18 times higher as that of modes 0, 1 and 2
3. Pulse frequencies are based on nominal device gain
4. Pulse widths are based on nominal oscillator frequency

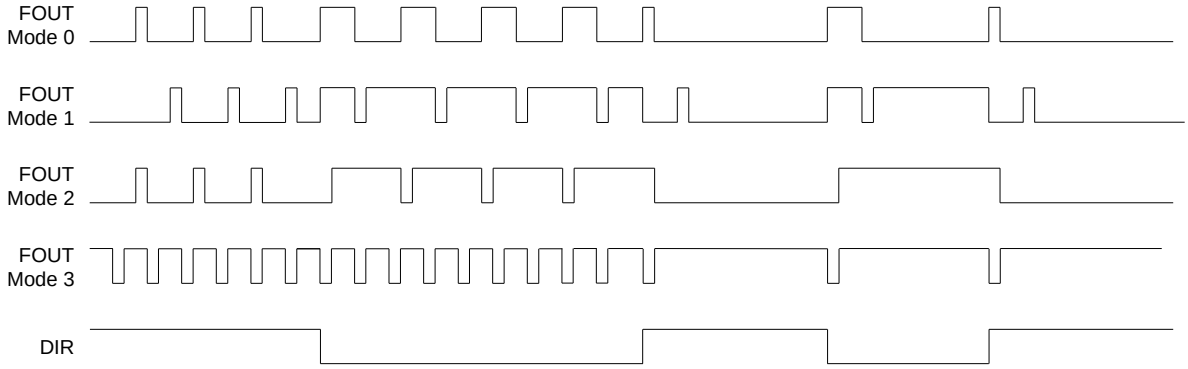


Figure 8: FOUT pulse output waveform (MS = V_{SS})

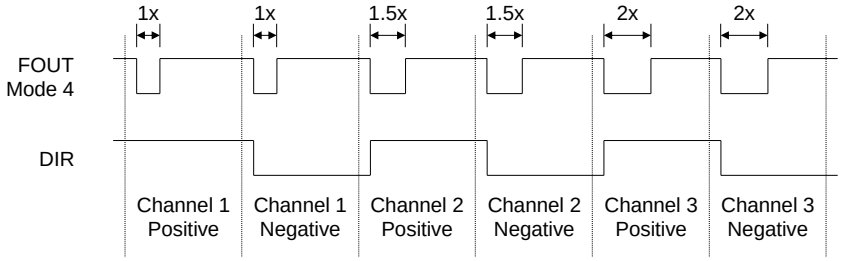


Figure 9: Details on FOUT pulse waveform in mode 4

Direction Output (DIR)

The SA4305A provides information on the direction of energy flow of the output pulses by means of the direction output. A logic low on the DIR output means that the output pulses represent negative energy and a logic high indicates positive energy. The direction output is only updated with each output pulse. The power-up state of the DIR output is logic high until the first output pulse is produced. The absolute energy sum mode ignores the energy direction prior to addition of the three device channels. Therefore the DIR output is not functional in absolute sum mode and will always be logic high. Figure 8 and Figure 9 illustrate the operation of the DIR output.

TYPICAL APPLICATION

The following description outlines the basic process required to design a typical three phase energy metering application using the SA4305A. The application is a 3-phase 4-wire configuration capable of measuring 3x220V/60A/50Hz with a precision better than Class 1.

The most important external circuits required for the SA4305A are the current input networks, the voltage input networks as well as the bias resistor. All resistors should be 1% metal film resistors of the same type to minimize temperature effects.

Bias Resistor

A bias resistor of R34 = 47kΩ sets optimum bias and reference currents on chip. Calibration of the meter should be done using the voltage inputs and not by means of the bias resistor.

Current Input Networks

Three current transformers are used to measure the three line currents. The output of each current transformer is terminated with a low impedance resistor split into two equal parts to obtain purely differential current input signals. The voltage across the termination resistors is converted to the required differential input currents through the current input resistors. Anti-alias filters are incorporated on these input resistors to filter any high frequency signal components that could affect the performance of the SA4305A.

The voltage drop across the current transformer termination resistors at maximum rated current should be in the order of 100mV$_{RMS}$. The current transformers have a low phase shift and a turns ratio of 1:2500. The value of the termination resistors R1, R2 is therefore

$$R1 = R2 = 100mV \times \frac{N_{CT}}{I_{MAX}} \times \frac{1}{2} \approx 2\Omega = R_B$$

where N_{CT} is the current transformer ratio (2500) and I_{MAX} is the maximum input current (60A).

The four current input resistors (R3, R4, R5, R6) should be of equal size to optimize the input networks low pass filtering characteristics, so the values can be calculated as follows:

$$R3 = R4 = R5 = R6 = \frac{I_{MAX}}{N_{CT}} \times \frac{R_B}{2 \times 16\mu A} = 1.5k\Omega = R_C$$

For optimum performance the cut-off frequency of the anti-alias filter should be between 10kHz and 20kHz. The equivalent resistance associated with each capacitor is $R_C/2$ so the capacitor values should be in the order of

$$C1 = C2 = \frac{1}{\pi f_{CI} R_C} = \frac{1}{\pi \times 10kHz \times 1.5k\Omega} \approx 22nF = C_C$$

where f_{CI} is the cut-off frequency of the anti-alias filter of the current input network.

The current input networks for channel 2 and channel 3 are identical.

Voltage Input Networks

The voltage sense inputs should optimally be set to an input current of $14\mu A_{RMS}$ at V_{NOM} (220V). The mains voltage is divided by means of a voltage divider to a lower voltage that is converted to the required input current by means of the input resistor. Once again an anti-alias filter is required to remove any high frequency signals that could affect the performance of the SA4305A. The phase shift of the current transformers is compensated by means of this anti-alias filter as well, by purposefully increasing the cut-off frequency.

The input resistor R22 sets the current input into the device. This resistor should not be too large else the capacitor for the anti-alias filter will be quite small which could cause inaccurate phase shift due to parasitic capacitances. Therefore R22 = 100kΩ is chosen and the voltage at the centre of the trimpot should be 1.4V (14µA x 100kΩ). The calibration range of the voltage input network should be about ±15% to ensure that all component tolerances can be catered for, so the total tuning range can be set to ±0.22V. Therefore the voltage across the trimpot and R23 is 1.62V. Choosing a 1kΩ trimpot results in

$$R23 = \frac{1k\Omega}{(2 \times 0.22)} \times (1.62 - 2 \times 0.22) \approx 2.7k\Omega$$

The effect of R22 can be ignored in the above equation, given the fact that R22 is significantly larger than P1 and R23. Now let R_A = R19 + R20 + R21 and

$$R_A = (P1 + R23) \times \left(\frac{220V}{1.62V} - 1\right) \approx 499k\Omega$$

so choose R19 = R20 = 200kΩ and R21 = 100kΩ.

The cut-off frequency of the anti-alias filter is adjusted so that the phase shift of the voltage input network is identical to the sum of the phase shifts of the current transformer and the current input network. The phase shift of the current input network is

$$\phi_{II} = -\tan^{-1}(\pi R_C C_C \times 50Hz) \approx -0.297°$$

The phase shift required on the voltage input network is therefore

$$\phi_{IV} = \phi_{II} - \phi_{CT} = -0.297° + 0.09° = -0.207°$$

where ϕ_{CT} is the phase shift of the current transformer which is typically about 0.09 degrees for a good quality current transformer. Neglecting R19, R20, R21 and R22 because all these resistors are significantly larger than P1 and R23 the capacitance required to achieve the -0.207 degree phase shift is

$$C7 = \frac{|\tan \phi_{IV}|}{2\pi(P1 + R23) \times 50Hz} \approx 3.3nF$$

resulting in a cut-off frequency of

$$f_{CV} = \frac{1}{2\pi(P1 + R23) \times C7} \approx 13kHz$$

The value of the cut-off frequency of the voltage input network is less critical than that of the current input network because the dynamic range of the voltage input is small. A cut-off frequency between 10kHz and 25kHz is acceptable.

The voltage input networks for channel 2 and channel 3 are identical

Device Setup

Depending on the desired output pulse format the four device setup pins (PGM0, PGM1, MS and FPM) need to be configured. These pins should be connected directly to either V_{DD} or V_{SS}. The MS and FPM inputs have internal pull-down resistors and may therefore be left floating. This will be equivalent to connecting the pin to V_{SS}. The TEST pin should be left floating.

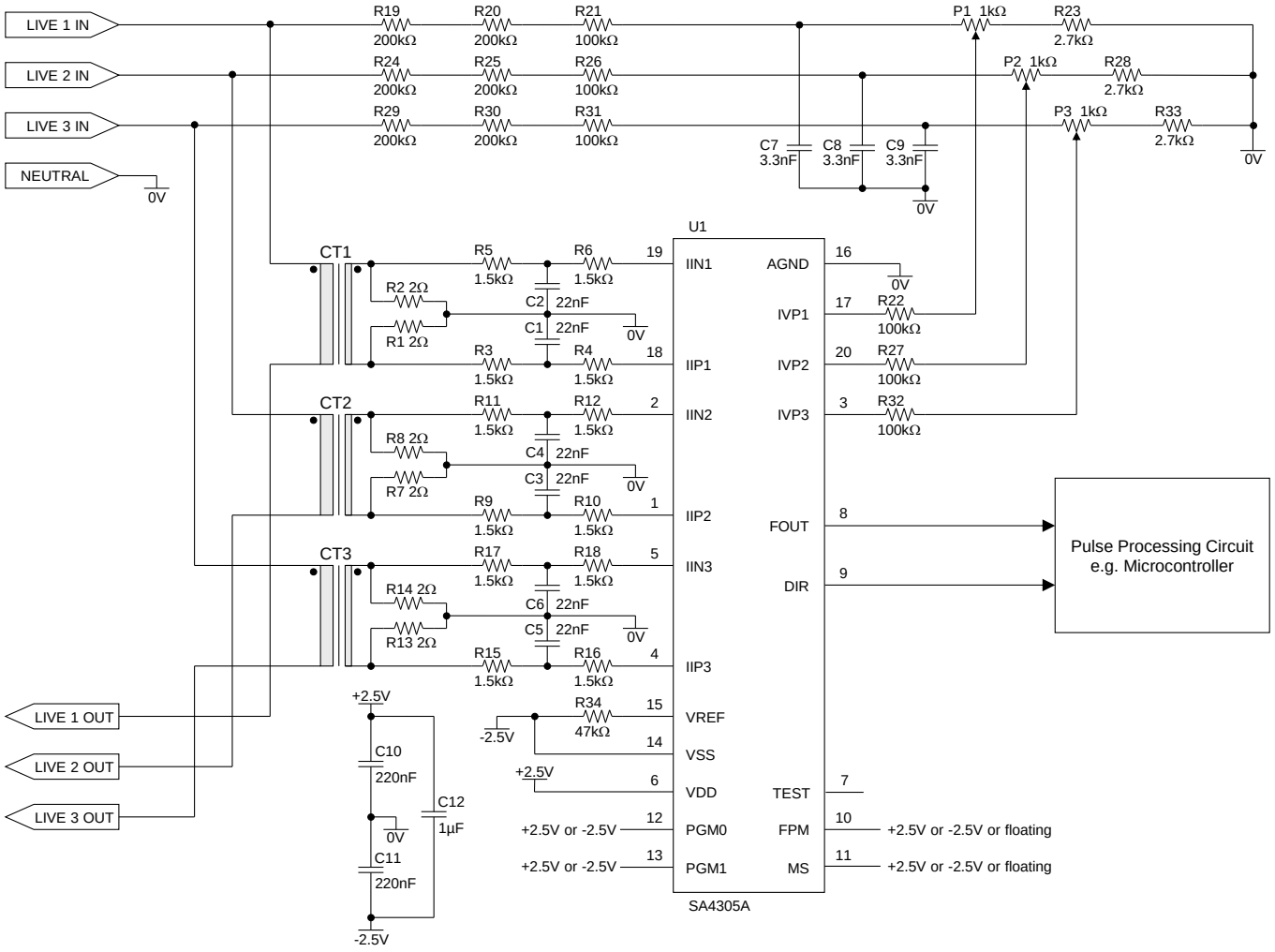


Figure 10: Typical application circuit

Table 2: Component list for typical application

Symbol	Description
U1	Energy metering device, SA4305ASAR
R1, R2, R7, R8, R13, R14	Resistor, 2Ω, 1%, metal film
R3, R4[1], R5, R6[1], R9, R10[1], R11, R12[1], R15, R16[1], R17, R18[1]	Resistor, 1.5kΩ, 1%, metal film
R19, R20, R24, R25, R29, R30	Resistor, 200kΩ, 1%, metal film
R21, R22[1], R26, R27[1], R31, R32[1]	Resistor, 100kΩ, 1%, metal film

Symbol	Description
R23, R28, R33	Resistor, 2.7kΩ, 1%, metal film
R34[1]	Resistor, 47kΩ, 1%, metal film
P1, P2, P3	Trim-pot, 25 turns, 1kΩ
C1, C2, C3, C4, C5, C6	Capacitor, 22nF, ceramic
C7, C8, C9	Capacitor, 3.3nF, ceramic
C10[2], C11[2]	Capacitor, 220nF, ceramic
C12[2]	Capacitor, 1µF, ceramic
CT1, CT2, CT3	Current transformer, 60A, 1:2500

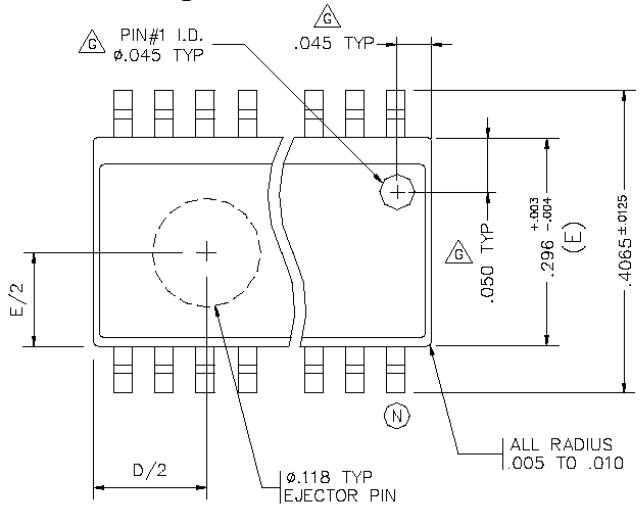
Note 1: Resistors R4, R6, R10, R12, R16, R18, R22, R27, R32 and R34 must be positioned as close as possible to the respective device pins

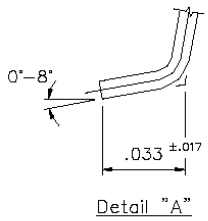
Note 2: Capacitors C10, C11 and C12 must be positioned as close as possible to the VDD and VSS power supply pins

PACKAGE DIMENSIONS

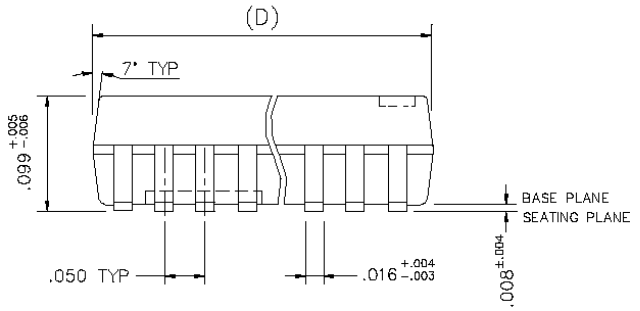
SOIC20 Package

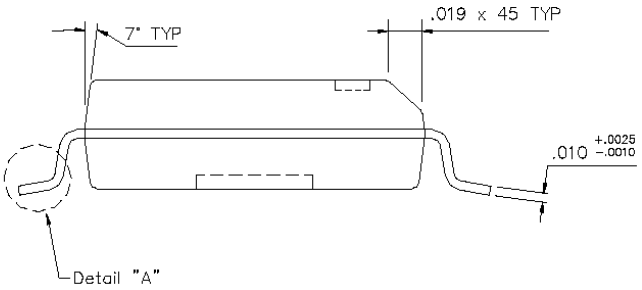
Dimensions are shown in inches





N	D VARIATIONS		
	MIN	NOM	MAX
16	.398	.405	.412
18	.449	.456	.463
20	.496	.503	.510
24	.599	.606	.613
28	.697	.704	.711





NOTES

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