Single Channel Single Phase Bidirectional Energy Metering IC with Instantaneous Frequency Output

SA4120A

FEATURES

- Meets the IEC62053, CBIP-88 and IS137799-1999 specification requirements for Class 1 AC static watt-hour meters for active energy
- Pulse output supplies instantaneous active power information
- Bidirectional power and energy measurement
- Adaptable to different types of current sensors
- Precision on-chip oscillator (70ppm/°C drift)
- Precision on-chip voltage reference (10ppm/°C drift)
- Integrated anti-creep function
- Low power consumption (<20mW typical)
- Measures AC inputs only
- Functionally compatible with SA2002H

DESCRIPTION

The SA4120A is an accurate single phase power/energy metering integrated circuit providing a single chip solution for single phase energy metering. Very few external components are required and the SA4120A does not require an external crystal or voltage reference. A precision oscillator and a precision voltage reference to supply the circuitry with a stable frequency and stable reference currents are integrated on the chip.

The SA4120A metering integrated circuit generates a pulse output, the frequency of which is proportional to the instantaneous active power consumption. The pulse output is intended to interface with a microcontroller or similar pulse counting circuitry. The SA4120A includes an anti-creep feature preventing any creep effects in the meter under no-load conditions.

The SA4120A integrated circuit is available in 8 pin dual inline (PDIP8) as well as 20 pin and 16 pin small outline (SOIC20, SOIC16) RoHS compliant package options.

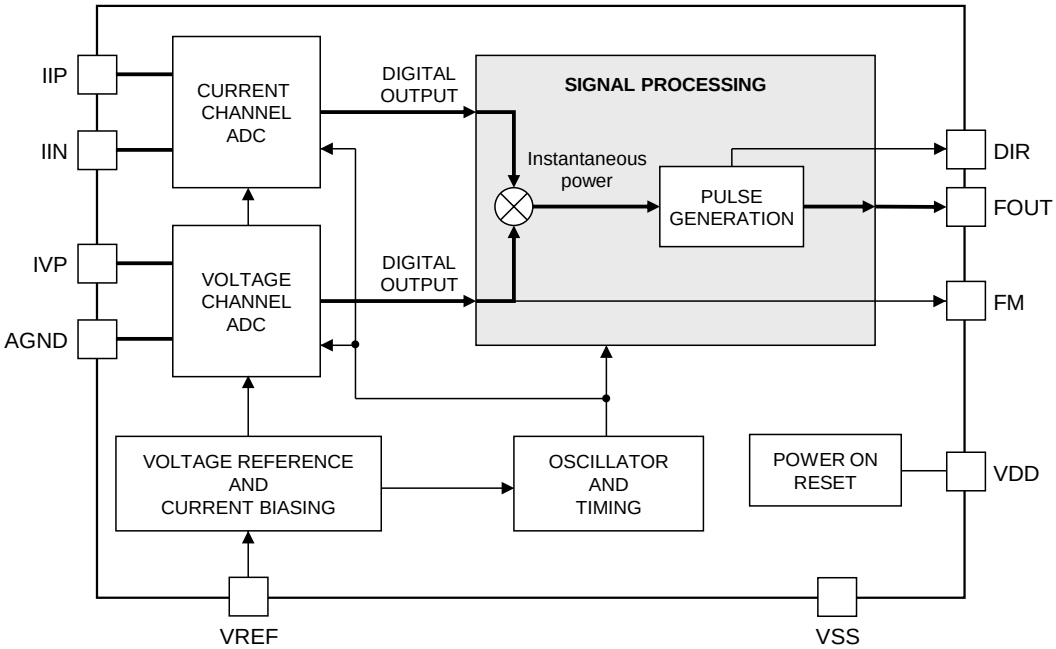


Figure 1: Block diagram

*FMO and DIR not available in PDIP8 package type

ELECTRICAL CHARACTERISTICS

(V_{DD} - V_{SS} = 5V ± 10%, over the temperature range -40°C to +85°C, unless otherwise specified. Refer to Figure 2 “Test circuit for electrical characteristics”.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
General						
Supply Voltage: Positive	V_{DD}	2.25	2.5	2.75	V	With respect to AGND
Supply Voltage: Negative	V_{SS}	-2.75	-2.5	-2.25	V	With respect to AGND
Supply Current: Positive	I_{DD}		3.5	4.5	mA	
Supply Current: Negative	I_{SS}		-3.5	-4.5	mA	
Analog Inputs						
Current Sensor Inputs (Differential)						
Input Current Range	IR_{IIP}, IR_{IIN}	-25		25	µA	Peak value
Offset Voltage	VO_{IIP}, VO_{IIN}	-4		4	mV	With R = 4.7kΩ connected to AGND
Voltage Sensor Inputs (Asymmetrical)						
Input Current Range	IR_{IVP}	-25		25	µA	Peak value
Offset Voltage	VO_{IVP}	-4		4	mV	With R = 4.7kΩ connected to AGND
Digital Outputs						
FOUT Output Frequency	F_{MAX}	1.04	1.16	1.25	kHz	At rated input conditions: 14µA_{RMS} on voltage channel, 16µA_{RMS} on current channel
FOUT, DIR, FMO Output High Voltage Output Low Voltage	 V_{OH} V_{OL}	 V_{DD}-1		 V_{SS}+1	 V V	 I_{SOURCE} = 5mA I_{SINK} = 5mA
On-chip Voltage Reference						
Reference Voltage	V_R	1.15	1.20	1.25	V	
Reference Current	$-I_R$	24.4	25.5	26.6	µA	With R = 47kΩ connected to V_{SS}
Temperature Coefficient	TC_R		10	70	ppm/ºC	
On-chip Oscillator						
Oscillator Frequency	f_{OSC}	3.15	3.57	4.00	MHz	
Temperature Coefficient	TC_{OSC}		70	200	ppm/ºC	

During manufacturing, testing and shipment we take great care to protect our products against potential external environmental damage such as Electrostatic Discharge (ESD). Although our products have ESD protection circuitry, permanent damage may occur on products subjected to high-energy electrostatic discharges accumulated on the human body and/or test equipment that can discharge without detection. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality during product handling.

ATTENTION: Electrostatic sensitive device. Requires special handling.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD} - V_{SS}		6	V
Current on any Pin	I_{PIN}	-150	150	mA
Storage Temperature	T_{STG}	-60	+125	ºC
Specified Operating Temperature Range	T_O	-40	+85	ºC
Limit Range of Operating Temperature	T_{limit}	-40	+85	ºC

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operational sections of this specification, is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

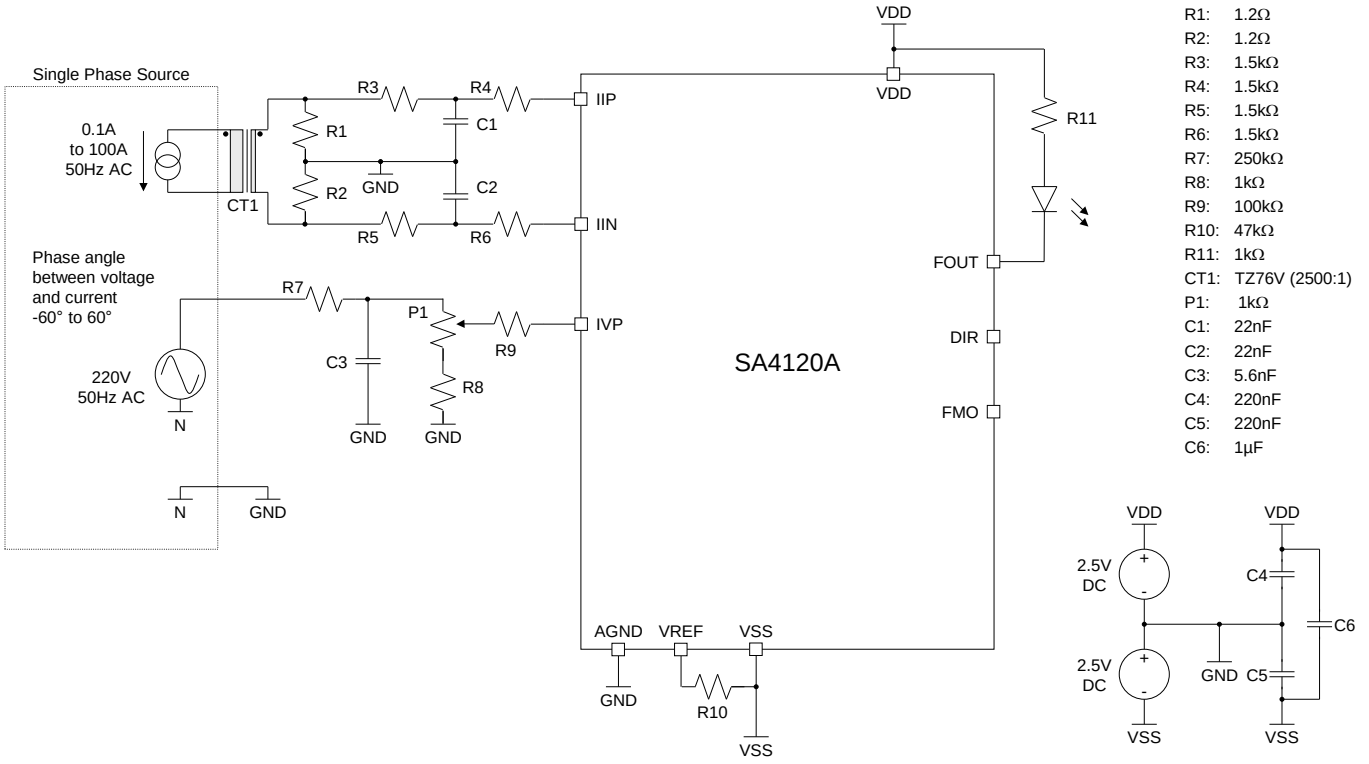


Figure 2: Test circuit for electrical characteristics

PIN DESCRIPTION

Designation	8 Pin	16 Pin	20 Pin	Description
AGND	8	16	20	Analog Ground. This is the reference pin for the current and voltage signal sensing networks. The supply voltage to this pin should be mid-way between V_{DD} and V_{SS}.
VDD	4	5	8	Positive Supply Voltage. The voltage to this pin should be +2.5V ± 10% with respect to AGND.
VSS	6	9	14	Negative Supply Voltage. The voltage to this pin should be -2.5V ± 10% with respect to AGND.
IVP	7	15	19	Analog Input for Voltage. The maximum current into the voltage sense input IVP should not exceed $16\mu A_{RMS}$. At nominal voltage an input current of $14\mu A_{RMS}$ is recommended. The voltage sense input saturates at an input current of ±25µA peak.
IIP, IIN	2, 1	2, 1	2, 1	Analog Inputs for Current. The maximum current into the current sense inputs IIP/IIN should be set at $16\mu A_{RMS}$. The current sense inputs saturate at an input current of ±25µA peak.
VREF	3	3	3	This pin provides the connection for the reference current setting resistor. A 47kΩ resistor connected to V_{SS} sets the optimum operating conditions.
DIR		7	13	Direction Indicator output. This output indicates the direction of energy flow.
FOUT	5	6	12	Pulse output. Refer to the Pulse Output section for information on the pulse output.
FMO		11	15	Mains Voltage Crossover output. This output indicates the polarity of the mains voltage.
NC		4, 8, 10, 12-14	4-7, 9-11, 16-18	No connection, leave unconnected.

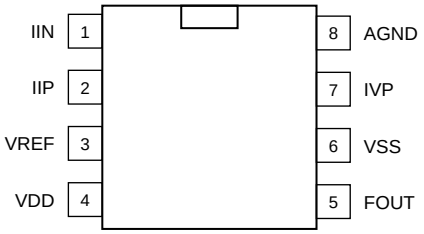


Figure 3: Pin connections for PDIP8 package

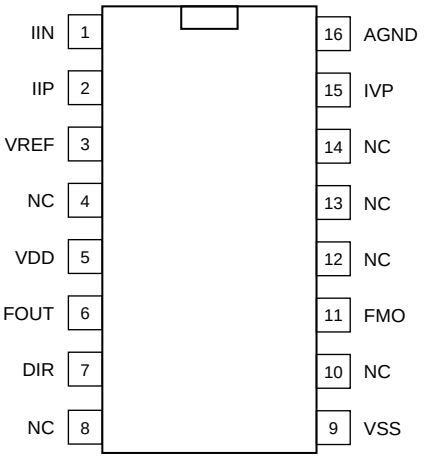


Figure 4: Pin connections for SOIC16 package

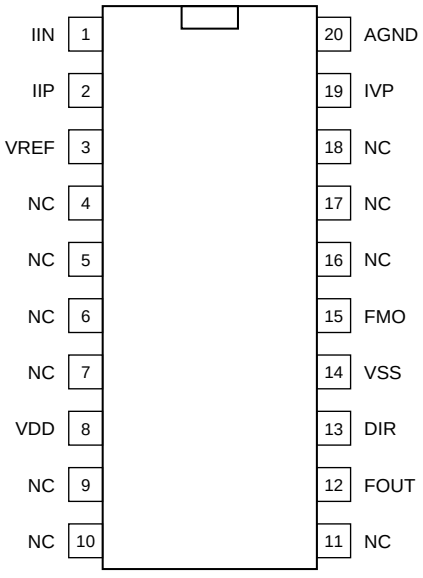


Figure 5: Pin connections for SOIC20 package

ORDERING INFORMATION

Part Number	Package
SA4120APAR-8	PDIP8 (RoHS compliant)
SA4120ASAR-16	SOIC16 (RoHS compliant)
SA4120ASAR-20	SOIC20 (RoHS compliant)

TERMINOLOGY

Anti-Creep Threshold

The anti-creep threshold is defined as the minimum energy threshold below which no energy is registered and therefore no pulses are generated on the pulse output.

Positive Energy

Positive energy is defined when the phase difference between the input signals IIP and IVP is less than 90 degrees (-90..90 degrees).

Negative Energy

Negative energy is defined when the phase difference between the input signals IIP and IVP is greater than 90 degrees (90..270 degrees).

Percentage Error*

Percentage error is given by the following formula:

$$\%Error = \frac{Energy\ registered - True\ Energy}{True\ Energy} \times 100$$

NOTE: Since the true value cannot be determined, it is approximated by a value with a stated uncertainty that can be traced to standards agreed upon between manufacturer and user or to national standards.

Rated Operating Conditions*

Set of specified measuring ranges for performance characteristics and specified operating ranges for influence quantities, within which the variations or operating errors of a meter are specified and determined.

Specified Measuring Range*

Set of values of a measured quantity for which the error of a meter is intended to lie within specified limits.

Specified Operating Range*

A range of values of a single influence quantity, which forms a part of the rated operating conditions.

Limit Range of Operation*

Extreme conditions which an operating meter can withstand without damage and without degradation of its metrological characteristics when it is subsequently operated under its rated operating conditions.

Maximum Rated Mains Current (I_{MAX})

Maximum rated mains current is the specified maximum current flowing through the energy meter at rated operating conditions.

Constant*

Value expressing the relation between the active energy registered by the meter and the corresponding value of the test output. If this value is a number of pulses, the constant should be either pulses per kilowatt-hour (imp/kWh) or watt-hours per pulse (Wh/imp).

Nominal Mains Voltage (V_{NOM})

Nominal mains voltage (V_{NOM}) is the voltage specified for the energy meter at rated operating conditions.

Maximum Output Frequency (F_{MAX})

The maximum output frequency (F_{MAX}) is the output frequency when 14μA_{RMS} and 16μA_{RMS} input current with zero phase shift are applied to the voltage and current inputs respectively. Both the voltage and current inputs saturate at an input current magnitude of 25μA, or at 17.68μA_{RMS} when using sine waves. The maximum input current on any channel is therefore defined to be 16μA_{RMS}, which leaves about 10% headroom to the saturation point. An additional headroom of 15% is reserved on the voltage channel to account for mains voltage fluctuations. The nominal output frequency of 1160Hz is achieved under such conditions.

* IEC 62052-11, 2003. Electricity Metering Equipment (AC) – General Requirements, Test and Test Conditions – Part 11: Metering Equipment

PERFORMANCE GRAPHS

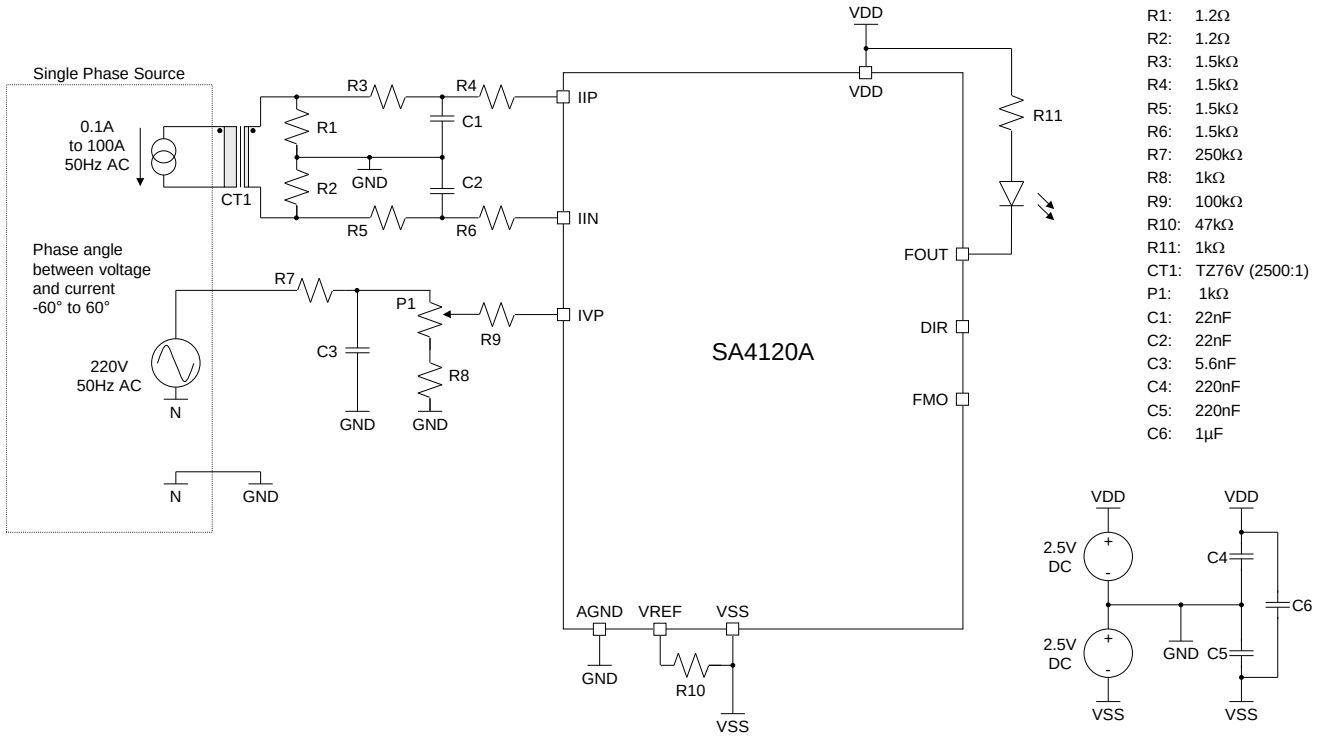
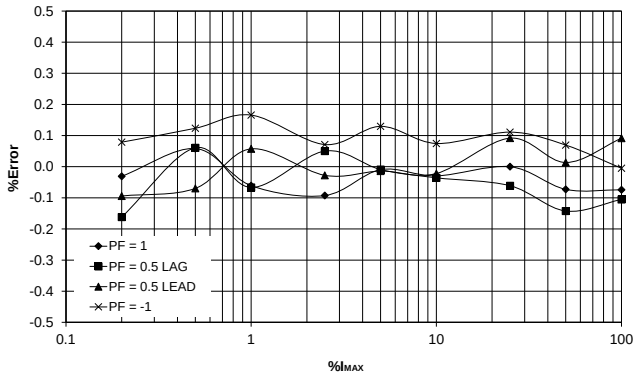
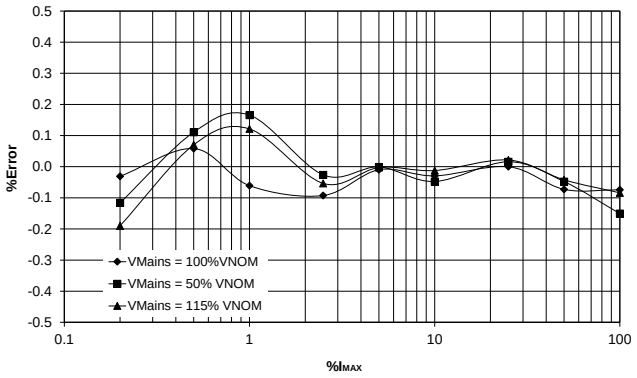


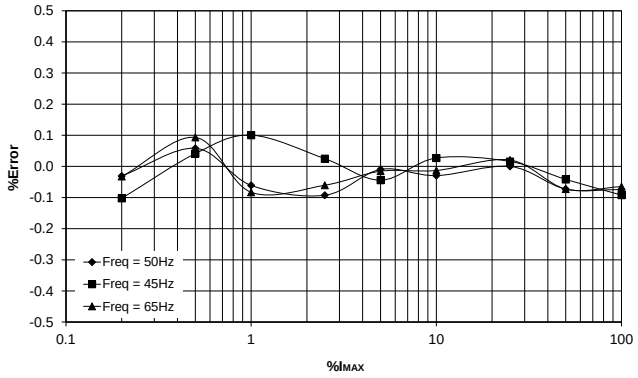
Figure 6: Test circuit for performance graphs



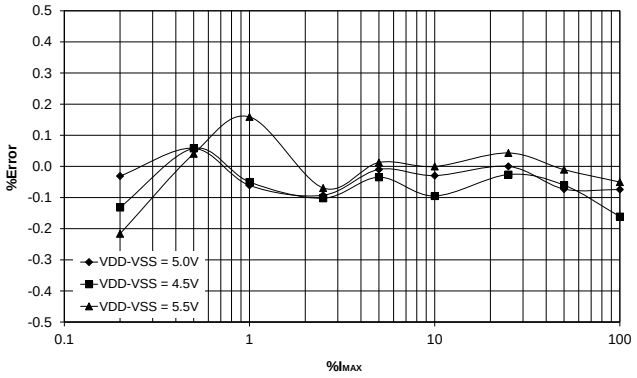
Graph 1: Freq = 50Hz, VMains = V_{NOM}, Temp = 25°C, V_{DD}-V_{SS} = 5.0V



Graph 2: PF = 1, Freq = 50Hz, Temp = 25°C, V_{DD}-V_{SS} = 5.0V



Graph 3: PF = 1, VMains = V_{NOM}, Temp = 25°C, V_{DD}-V_{SS} = 5.0V



Graph 4: PF = 1, Freq = 50Hz, VMains = V_{NOM}, Temp = 25°C

FUNCTIONAL DESCRIPTION

Theory of Operation

The SA4120A includes all the required functions for single channel single phase power and energy measurement. Two AD converters sample the voltage and current input signals. The two digital signals, accurately representing the voltage and current inputs, are multiplied using digital multiplication. The output of the multiplier represents the instantaneous power. The pulse generation circuit creates a pulse output where the instantaneous frequency is proportional to the instantaneous power measured.

For given voltage and current signals the instantaneous power is calculated by:

$$p(t) = v(t) \times i(t)$$
$$p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \psi)$$

Let $\phi = \theta - \psi$, and $V_{RMS} = \frac{V_M}{\sqrt{2}}$ and $I_{RMS} = \frac{I_M}{\sqrt{2}}$ then

$$p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \theta - \phi)$$
$$p(t) = V_{RMS} I_{RMS} (\cos\phi + \cos(2(\omega t + \theta) - \phi))$$

where
p(t) is the instantaneous power,
v(t) is the instantaneous voltage signal,
i(t) is the instantaneous current signal,
V_M is the amplitude of the voltage signal,
I_M is the amplitude of the current signal,
θ is the phase angle of the voltage signal and
ψ is the phase angle of the current signal.

The instantaneous power output is integrated over time to obtain the output energy by simply counting the output pulses. This removes the double mains frequency component cos(2(ωt+θ)-ϕ) and the average pulse output rate is therefore equivalent to

$$P = \frac{1}{T}\int_0^T p(t)dt$$
$$P = V_{RMS} I_{RMS} \cos\phi$$

where
P is the average power and
$cos\phi$ is the power factor.

Linearity

The SA4120A is a CMOS integrated circuit, which performs power/energy calculations across a dynamic range of 500:1 to an accuracy that exceeds the IEC62053 specification.

Analog Inputs

The input circuitry of the current and voltage sensor inputs is illustrated in Figure 7. These inputs are protected against electrostatic discharge through clamping diodes. The feedback loops from the outputs of the amplifiers A_I and A_V generate virtual short circuits between IIP and IIN as well as IVP and AGND. The current sense inputs (IIP and IIN) are identical and balanced. The AD converters convert the signals on the voltage and current sense inputs to a digital format for further processing. All internal offsets are eliminated through the use of various cancellation techniques.

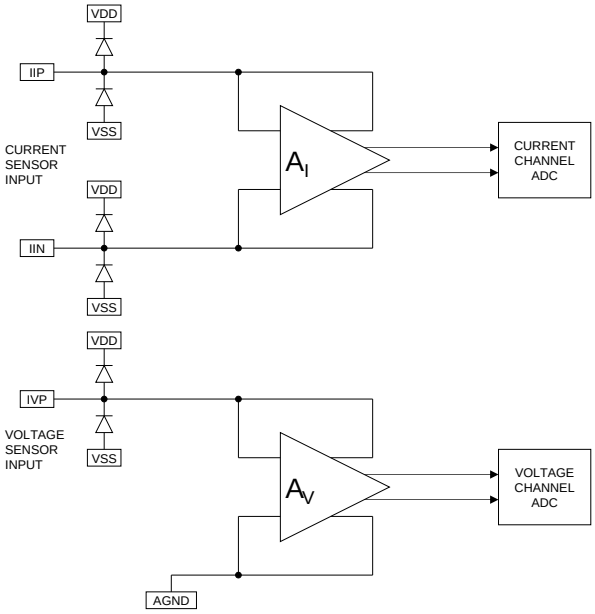


Figure 7: Analog input configuration

Digital Outputs

The calculations required for power and energy are performed and the result is converted to pulses on the FOUT pulse output. The instantaneous output frequency on the pulse output is proportional to the instantaneous active power consumption measured. The pulse output is intended for interfacing the SA4120A to a microcontroller or similar pulse processing circuit.

Anti-Creep Threshold

An integrated anti-creep function prevents any output pulses from appearing on the pulse output if the energy measured is less than 0.02% of F_{MAX}, where F_{MAX} is the energy registered when the input currents for voltage and current are 14μA_{RMS} and 16μA_{RMS} with zero phase shift respectively.

Reverse Energy Flow Indication

The SA4120A assesses the phase difference between the voltage and current channel signals. If this phase difference is greater than 90 degrees then the reverse energy indicator is activated. This facility is designed to detect the wrongful connection or possible tampering of the meter. The operation of the direction output is fully described in the Output Signals section.

Starting Current

The SA4120A generates pulses on the pulse output for an input power greater than 0.02% of F_{MAX}. This is to comply with the IEC requirement where the meter is required to generate pulses for currents greater than 0.4%Ib.

Power-On Reset

The SA4120A has a power-on reset circuitry that activates whenever the voltage between VDD and VSS is less than 3.6V ± 8%.

Power Consumption

The power consumption of the SA4120A integrated circuit is less than 25mW.

Compatibility with SA2002H

The SA4120A can be used as a functionally compatible replacement for the SA2002H. It should however be noted that the value of the reference resistor on the VREF pin has to be changed from 24kΩ to 47kΩ.

INPUT SIGNALS

Voltage Reference (VREF)

A bias resistor of 47kΩ sets optimum bias and reference conditions on chip. Calibration of the SA4120A should be done on the voltage input and not on the VREF input.

Current Sense Inputs (IIP and IIN)

Figure 8 shows the typical connections for a current sensor input when using a shunt or a current transformer as a current sensing element. A typical single channel meter can be designed with either a current transformer or a shunt resistor as a current sensing element. At maximum rated mains current (I_{MAX}) the resistor values should be selected for an input current of 16µA$_{RMS}$. The current sense inputs saturate at an input current of ±17.6µA$_{RMS}$ (±25µA$_{PEAK}$), so this allows about 10% headroom until saturation occurs.

For a current transformer application the resistors RA and RB form the termination resistor. The reference level is connected in the centre of the termination resistor to achieve purely differential input currents. The voltage drop across the termination resistors at maximum rated mains current (I_{MAX}) should be in the order of 100mV$_{RMS}$. The termination resistance should also be significantly smaller than the DC resistance of the current transformers secondary winding.

When using a shunt resistor as a current sensing element the voltage drop across the shunt resistor RSH at maximum rated mains current (I_{MAX}) should not be less than 5mV$_{RMS}$ and not exceed 100mV$_{RMS}$.

The resistors R1 to R4 define the current flowing into the device. For best performance the SA4120A requires anti-alias filters on the current sense inputs. These filters are realized by means of the capacitors C1 and C2. The typical cut-off frequency of these filters should be between 10kHz and 20kHz. The optimum input network is achieved by setting the input resistors equal, i.e. setting R1 = R2 = R3 = R4 = R_C. This sets the equivalent resistance associated with each capacitor to R_C/2.

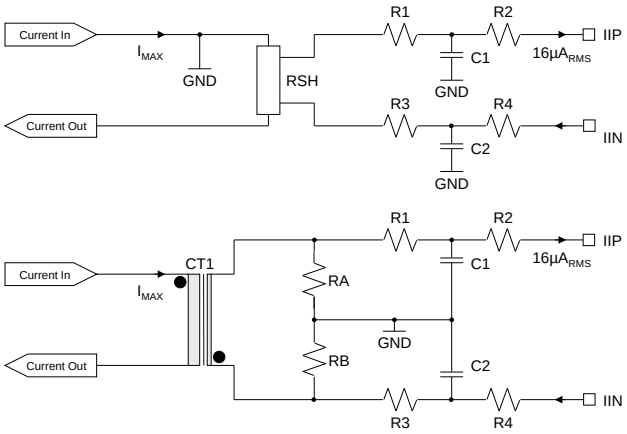


Figure 8: Current sense input configuration

Voltage Sense Input (IVP)

Figure 9 shows the voltage sense input configuration. The voltage sense input saturates at an input current of ±17.6µA$_{RMS}$ (±25µA$_{PEAK}$). The current into the voltage sense input should be set to 14µA$_{RMS}$ at nominal mains voltage (V_{NOM}) to allow for a mains voltage variation of up to +25% without saturating the voltage sense input.

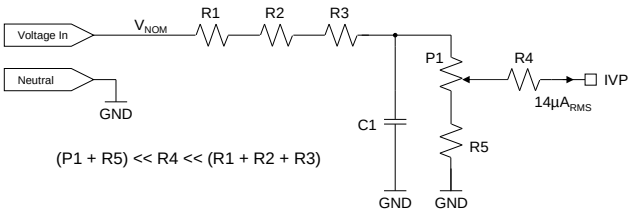


Figure 9: Voltage sense input configuration

For best performance the SA4120A also requires an anti-alias filter on the voltage sense input. Referring to Figure 9, the capacitor C1 is used to both implement the anti-alias filter as well as compensating for any phase shift caused by the current transformer or the shunt resistor. The resistor R4 defines the input current into the device. The optimum input network is achieved by setting R4 in the order of 100kΩ. If R4 is made too large the capacitor C1 will be very small and the accuracy of the phase compensation could be affected by stray capacitances. The potentiometer P1 is used for calibration purposes.

OUTPUT SIGNALS

Pulse Output (FOUT)

The average nominal output frequency of the pulse output is given by

$$f_{FOUT} = 1160 \times \left| \frac{IV \times II \times \cos\phi}{14 \times 16} \right| \quad \ldots(1)$$

where

IV and *II* are the analog input currents in μA_{RMS} on the voltage and current sense inputs and

ϕ = the phase angle between the current and voltage signals.

The integrated anti-creep threshold ensures that no output pulses are generated if the energy measured is below 0.02% of F_{MAX}, where F_{MAX} is the output frequency when the voltage and current channel receive input currents of $14\mu A_{RMS}$ and $16\mu A_{RMS}$ respectively. The power-up state of the pulse output is logic high.

Figure 10 shows the output waveform of FOUT. The output pulse width t_{LP} is 71μs at nominal on-chip oscillator frequency. The pulse width doubles in the case of reverse energy. This allows direct sensing of the energy direction without using the direction output.

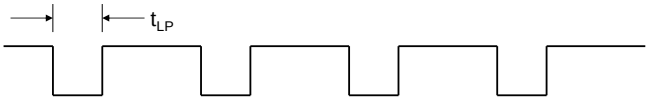


Figure 10: FOUT pulse output waveform

Direction Output (DIR)

The SA4120A provides information on the direction of energy flow by means of the direction output. A logic low in the DIR output means that the device measures negative energy and a logic high indicates positive energy. The direction output is only updated with each output pulse. The power-up state of the DIR output is logic low until the first output pulse is produced. This output pin is not available on the PDIP8 package option.

Mains Crossing Output (FMO)

The FMO pin indicates the polarity of the mains voltage signal and switches state at the mains voltage zero crossover. Due to comparator offsets, the duty cycle may not equal exactly 50%. The time between successive rising or falling edges is equal to the mains period. A microcontroller may use FMO to extract mains period information. The state of this pin is undetermined in the absence of a mains voltage. This output pin is not available on the PDIP8 package option.

TYPICAL APPLICATION

The following description outlines the basic process required to design a typical single phase energy meter using the SA4120A and a shunt resistor as a current sensing element. The meter is capable of measuring 220V/40A/50Hz with a precision better than Class 1.

The most important external circuits required for the SA4120A are the current input network, the voltage input network as well as the bias resistor. All resistors should be 1% metal film resistors of the same type to minimize temperature effects.

Bias Resistor

A bias resistor of R10 = 47kΩ sets optimum bias and reference currents on chip. Calibration of the meter should be done using the voltage input and not by means of the bias resistor.

Current Input Network

The voltage drop across the shunt resistor at maximum rated current should not be less than $5mV_{RMS}$ and not exceed $100mV_{RMS}$. A 320μΩ shunt is chosen which sets the voltage drop at maximum rated current to 12.8mV and the maximum power dissipation in the shunt to 0.5W. The voltage across the shunt resistor is converted to the required differential input currents through the current input resistors. Anti-alias filters are incorporated on these input resistors to filter any high frequency signal components that could affect the performance of the SA4120A.

The four current input resistors (R1, R2, R3, R4) should be of equal size to optimize the input networks low pass filtering characteristics, so the values can be calculated as follows:

$$R1 = R2 = R3 = R4 = I_{MAX} \times \frac{R_{SH}}{4 \times 16\mu A} = 200\Omega = R_C$$

For optimum performance the cut-off frequency of the anti-alias filter should be between 10kHz and 20kHz. The equivalent resistance associated with each capacitor is $R_C/2$ so the capacitor values should be in the order of

$$C1 = C2 = \frac{1}{\pi f_{CI} R_C} = \frac{1}{\pi \times 15kHz \times 200\Omega} \approx 100nF = C_C$$

where f_{CI} is the cut-off frequency of the anti-alias filter of the current input network.

Voltage Input Network

The voltage sense input requires an input current of 14μA$_{RMS}$ at V_{NOM} (220V). The mains voltage is divided by means of a voltage divider to a lower voltage that is converted to the required input current by means of the input resistor. Once again an anti-alias filter is required to remove any high frequency signals that could affect the performance of the SA4120A. A shunt typically has very little phase shift so phase compensation is not required.

The input resistor R8 sets the current input into the device. This resistor should not be too large else the capacitor for the anti-alias filter will be quite small which could cause inaccurate phase shift due to parasitic capacitances. Therefore R8 = 100kΩ is chosen and the voltage at the centre of the trimpot should be 1.4V (14μA x 100kΩ). The calibration range of the voltage input network should be about ±15% to ensure that all component tolerances can be catered for, so the total tuning range can be set to ±0.22V. Therefore the voltage across the trimpot and R9 is 1.62V. Choosing a 1kΩ trimpot results in:

$$R9 = \frac{1k\Omega}{(2 \times 0.22)} \times (1.62 - 2 \times 0.22) \approx 2.7k\Omega$$

The effect of R8 can be ignored in the above equation, given the fact that R8 is significantly larger than P1 and R9. Now let R_A = R5 + R6 + R7 and

$$R_A = (P1 + R9) \times \left(\frac{220V}{1.62V} - 1\right) \approx 499k\Omega$$

so choose R5 = R6 = 200kΩ and R7 = 100kΩ.

The cut-off frequency of the anti-alias filter is adjusted so that it is identical to that of the current input network anti-alias filters. This ensures that the phase shift caused by the anti-alias filters is identical on the current and voltage input networks. Therefore

$$\frac{1}{\pi C_C \times R_C} = \frac{1}{2\pi(P1 + R9) \times C3}$$

and so C3 = 2.7nF.

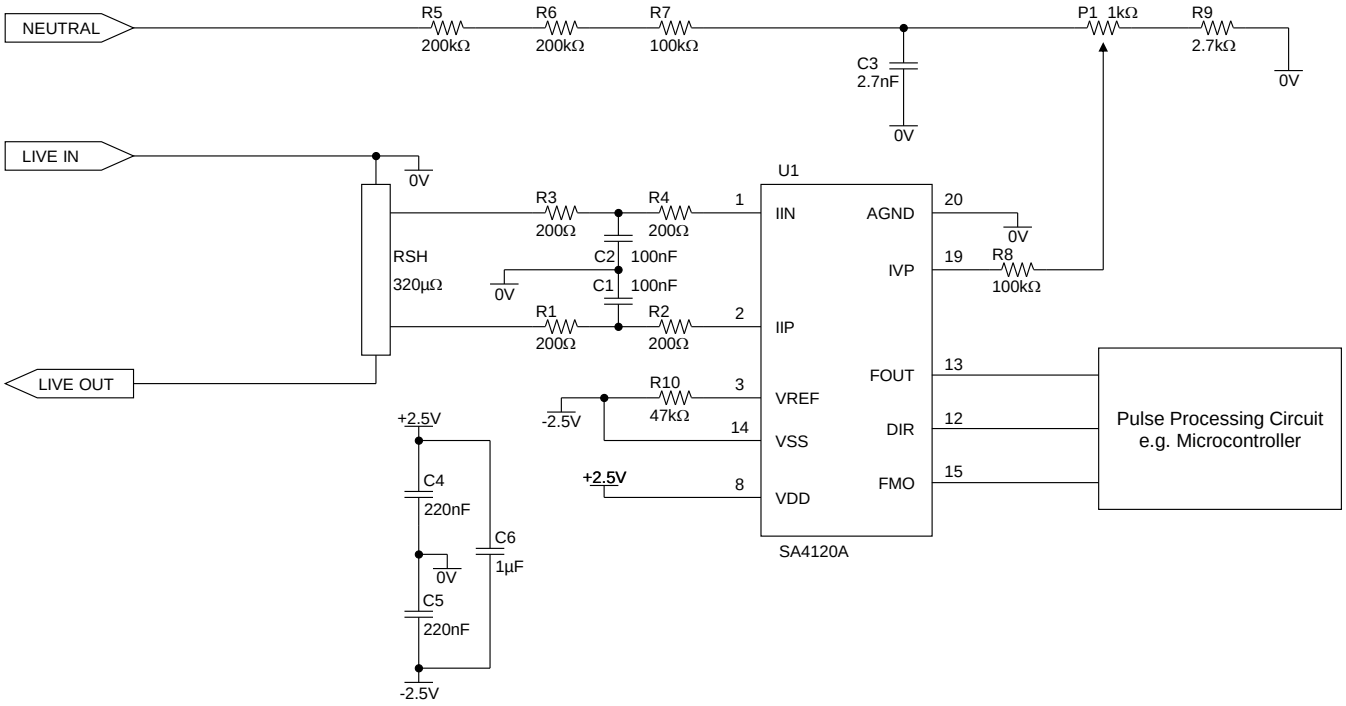


Figure 11: Typical application circuit

Table 1: Component list for typical application

Symbol	Description
U1	Energy metering device, SA4120ASAR-20
RSH	Shunt Resistor, 40A, 320μΩ
R1, R2[1], R3, R4[1]	Resistor, 200Ω, 1%, metal film
R5, R6	Resistor, 200kΩ, 1%, metal film
R7, R8[1]	Resistor, 100kΩ, 1%, metal film

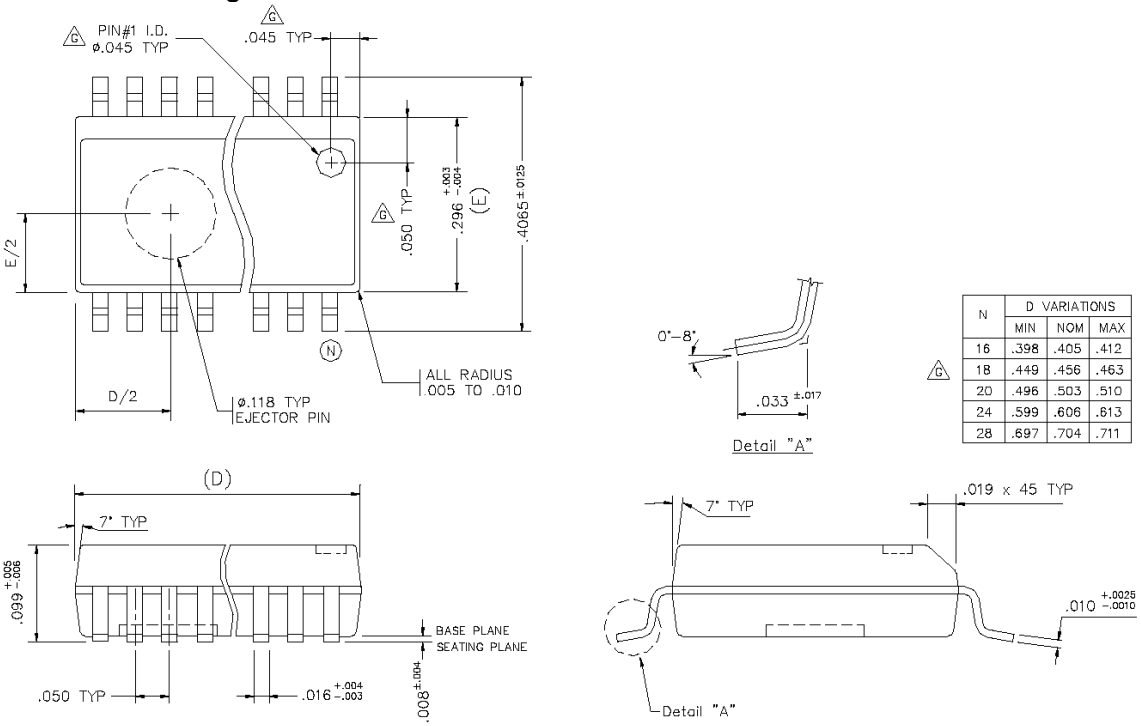
Symbol	Description
R9	Resistor, 2.7kΩ, 1%, metal film
R10[1]	Resistor, 47kΩ, 1%, metal film
P1	Trim-pot, 25 turns, 1kΩ
C1, C2	Capacitor, 100nF, ceramic
C3	Capacitor, 2.7nF, ceramic
C4[2], C5[2]	Capacitor, 220nF, ceramic
C6[2]	Capacitor, 1μF, ceramic

Note 1: Resistors R2, R4, R8 and R10 must be positioned as close as possible to the respective device pins
Note 2: Capacitors C4, C5 and C6 must be positioned as close as possible to the VDD and VSS power supply pins

PACKAGE DIMENSIONS

SOIC16 and SOIC20 Packages

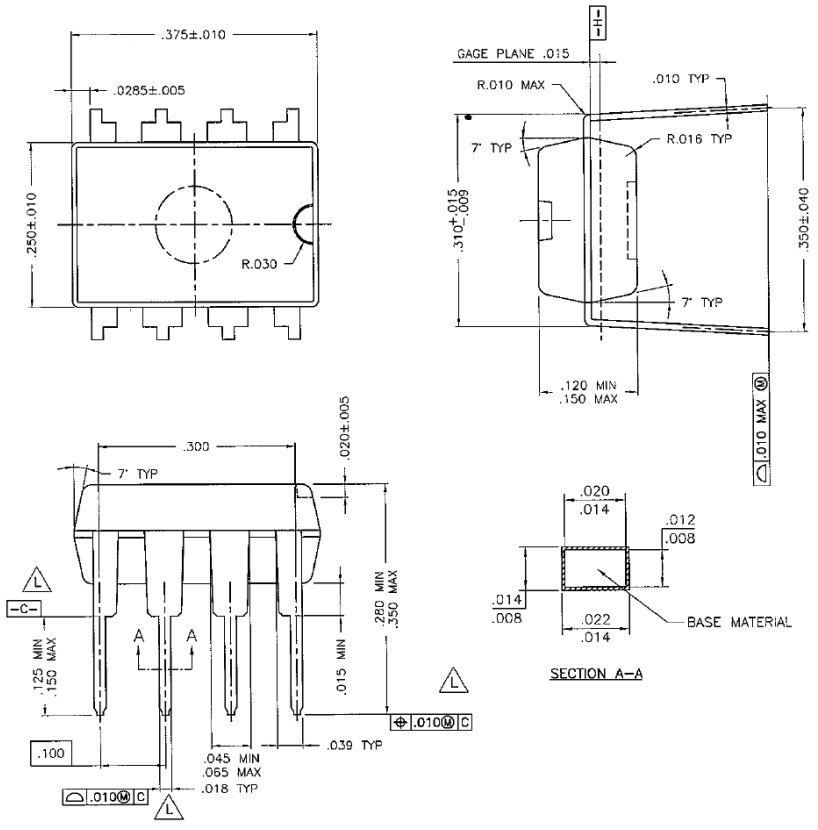
Dimensions are shown in inches



N	D VARIATIONS		
	MIN	NOM	MAX
16	.398	.405	.412
18	.449	.456	.463
20	.496	.503	.510
24	.599	.606	.613
28	.697	.704	.711

PDIP8 Package

Dimensions are shown in inches



NOTES

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